COMPUTE

Microprocessor Users Group Newsletter

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BLC I/O EXPANSION CARD

The BLC 508 Input/Output Expansion Card is the newest addition to National's Series/80 Board Level Computer series based on the 8080 microprocessor. The simple, cost effective board provides 8-bit parallel ports, four input and four output, and sells for $315 for 1-9, $189 in quantities of 100.

The board can transfer data at rates as high as 1.3 megabytes per port; the practical limit is set by the peripherals or I/O handling software. The board connects to the system bus through the 86-pin card edge, and has a 100-pin edge connector for parallel I/O. Data, address, and control signals are TTL compatible, and it operates on +5V DC. The four output ports have a variable width strobe available for peripherals, which is set in a range from 100 to 1600 nanoseconds by a convenient plug jumper on the board.

The block of port addresses is set by two rotating switches to one of 64 possible base addresses, and can be switch disabled. The board can accept eight external interrupt requests, which are buffered and passed onto the system bus. For more information contact Larry Choice, (408) 737-6592.

MICROCOMPUTERS UNDERWATER

Inspection of underwater pipe and oil drilling platforms, and searching for and retrieving objects from the ocean floor, present many problems. The main problem, of course, is man. Even equipped with elaborate life-support systems, the workday is limited, the costs are high, and the dangers great.

Hydro Products has an answer which is probably the next best thing to a porpoise with an engineering degree. It is a highly "intelligent", microcomputer-controlled undersea robot that has the eyes, ears and arms that give great flexibility in many applications. Called the RCV-150, it is probably the most sophisticated and flexible commercially-produced submersible in use today.

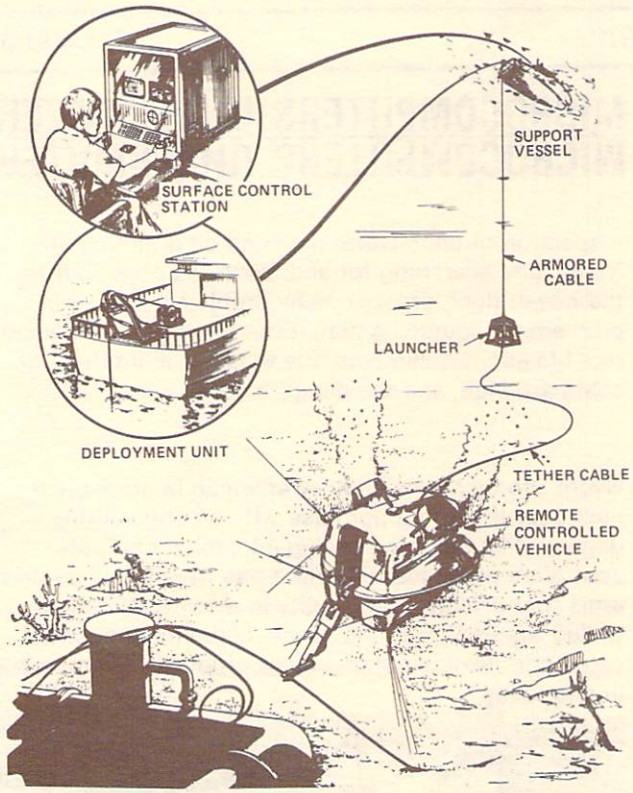
This robot, an undersea inspection and work system, incorporates a microcomputer.

The key to the design is a pair of identical PACE microcomputers from National. One is in the undersea vehicle, the other on the surface mother ship. Virtually all communications, display and control functions are managed by the microcomputers.

(continued overleaf)

Users Group Director ..... Georgia Marszalek
Applications Consultant ..... Keith Winter
Editor ..... David Graves
Associate Editor ..... Jim Teller
Sponsored by National Semiconductor Corporation, 2900 Semiconductor Drive, Santa Clara, California 95051

The undersea portion of the RCV-150 consists of a small cable-tethered vehicle. The vehicle's small size makes it easy to launch and retrieve while a large array of equipment gives the capability of much larger submersibles. Four 250-watt lamps provide illumination for the television camera.



Microprocessor-Controlled Remote Inspection and Work System

Only 50 percent of the available space in the vehicle is currently being used, allowing for the addition of marine magnetometers, acoustic trackers, sonar depth-finders, 35mm still cameras, search sonars, or even an additional manipulator arm should it be desired.

The software and firmware is designed to allow for additional features to meet future application requirements. Control firmware can be supplied on PROM for convenient field installation.

Internal depth and yaw programs referenced to depth and turn-rate signals are under PACE microcomputer control. This relieves the operator of many maneuvering tasks, allowing him to concentrate on observation, inspection, and manipulation duties.

Using the microcomputers has made system response faster. It turns smoothly and quickly and can stop on a dime. Since it automatically controls its own depth and heading, it can remain stationary in these axes without operator intervention.

PACE SYSTEM

Three PACE Board-Level Computer cards comprise the vehicle's microcomputer while the same three plus a second PROM board make up the surface control station microcomputer. The compact boards include the 16-bit PACE CPU, the 2K by 16-bit PACE PROM and the 1K by 16-bit PACE RAM.

The PROM memory firmware houses the operating programs for the vehicle and the control unit. The second PROM board in the control station contains the maintenance and self-test program and CRT display formats. The RAM boards temporarily store intermediate results during processing.

An array of standard sensors includes various depth, heading rate, roll, pitch and temperature sensors, and sea-water intrusion sensors. The temperature of the electronics package and hydraulic system is constantly monitored as a safety feature. Tools can be placed on the undersea vehicle, such as the three-foot long manipulator which has four degrees of freedom, a cable cutter, a soft-line cutter, cleaning brush, pinger dropper, and a grabber arm.

The surface-ship control station has two monitors; one shows the video pictures from the undersea television camera, while the other displays operations data. Selected data can be superimposed on the video channel annotating video tapes with position information, valuable in later review.

Illuminated bar graph displays, on the control station, indicate power levels and temperatures. Illuminated switches indicate control position and serve as warning annunciators. Problems in the vehicle are immediately reported to the operator by the RCV's microcomputer which continuously monitors vehicle performance.

The microcomputer in the control station scans the control panel 20-times-per-second. When a control maneuver is given by the operator, the signal is encoded and passed through a RF-telemetry data link via coaxial cable to the vehicle microprocessor. This microprocessor then interprets the command, activates the electrohydraulic servos which in turn, continuously solve the equations of motion at a rate of 30 times per second.

Data sensed by the vehicle sensors and detectors is transferred through the microprocessors for surface display.

One of the problems that had to be overcome in designing the new vehicle software system concerned the tight time constraints for program execution. It was first thought that a surface minicomputer would make the necessary equations-of-motion calculations and transmit the data to operate the RCV servos.

The data transmission system couldn't handle high-speed data rate from the mini to the vehicle. Using the microcomputer in the vehicle to perform its own calculations allows less complex data transmission and a more reliable system.

For additional information on this application contact:

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Fiber Optics Connector

by John T. Williams
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FABRICATION OF A FIBER INTERFACE

In designing a two-SC/MP microprocessor system it soon became apparent that some means for communication had to be developed that would permit transfer of data with the least noise. For my application, fiber optics was the best choice; however, it turned out that designing the emitter and receiver circuits was simpler than trying to make the interfaces to the fiber optics cable.

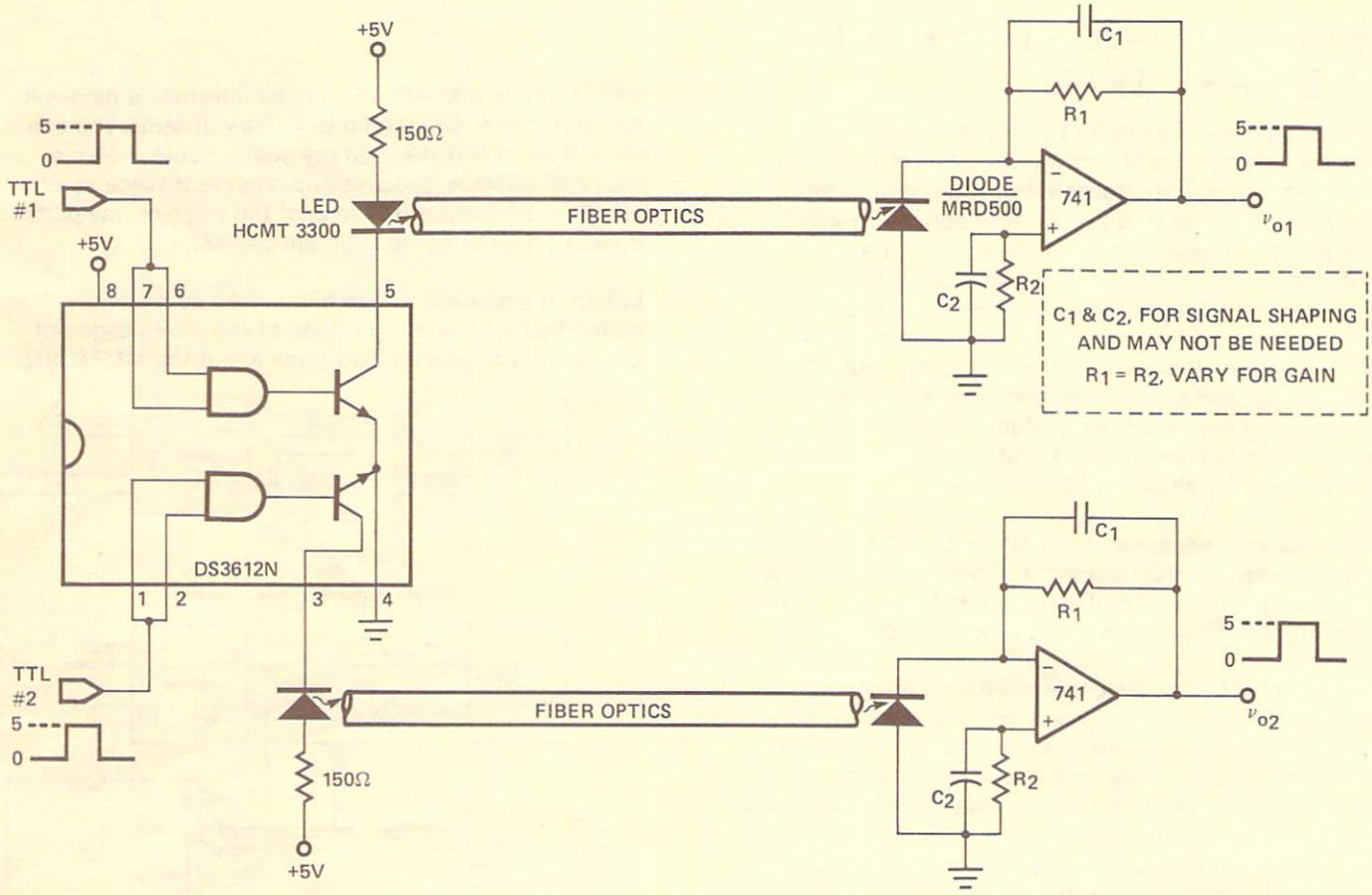
First, I found that manufactured connectors and cables were too expensive for me, and direct permanent installation would inhibit troubleshooting and setting up of the system in the application for the maximum transfer of light. What I found was an easy, low-cost connector method that gave me exceptional results. It consists of a BNC connector that is modified to hold the emitter (or receiver) and the fiber cable in a lightproof package. I used plastic fiber cables at $5.50 per 200 ft, LEDs for the emitter and photo-pin diodes for the receivers. The fibers were cut to length and the ends sanded smooth with 800 emery paper.

The LEDs were cut just shy of the source and polished with the same 800 emery paper. The pin diodes were sanded free of glass to the metal case and polished with 800 emery paper. When inserted into the BNC connector the fibers are prevented from shifting by the use of thin-wall shrink tubing. Replacement of any of the parts is simple and straightforward.

The following is a description of how to assemble the interface. Refer to the illustration for clarity.

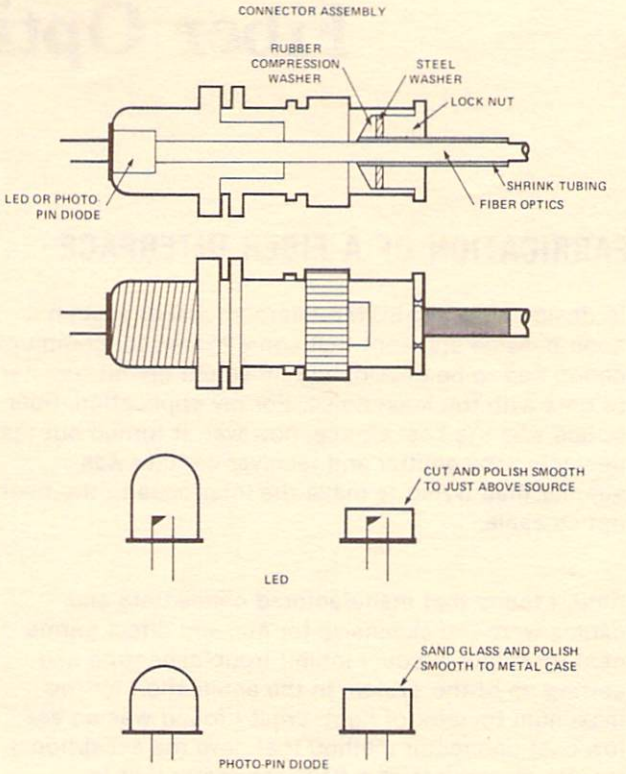
FABRICATING THE CONNECTOR

1. Assemble both the male and female halves of the connector and drill out the center pin.
2. Drill a hole, down the center, completely through the connector to a size that will just accommodate the fiber cable.



TYPICAL CIRCUIT WITH TWO CHANNELS

3. From the male end drill a concentric hole the diameter of the LED or diode. The device should fit in completely and snuggly on the walls when inserted.
4. With the device in its hole, insert the fiber cable from the opposite end until it butts up against the face of the device. Slip the shrink tubing on the fiber cable until it stops and protrudes from the end of the connector. Hold it in place while removing the cable and shrink it in place with just enough heat as not to damage the fibers.
5. Reinsert the cable, making certain it fits correctly, and then slip on the rubber compression washer, steel washer and locknut that is supplied with the BNC connector. Tighten the nut down until it prevents movement of the fiber cable.
6. Make sure that the connector separates and reconnects with ease. The fiber cable will extend through the end when separated.
7. Repeat this procedure, on the other end of the cable, with the other device. This method should supply you with a quick and easy cable assembly. I have found that if the signal isn't properly transmitted across this cable using LEDs, usually there isn't enough drive on the emitter, or the spectrum response of the receiver and emitter are not matched.



Connector Assembly

Applications Corner

SEVEN-SEGMENT TO BCD— THE EASY WAY

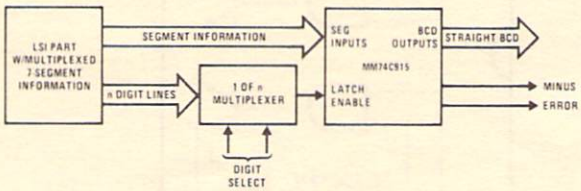
Many popular devices output multiplexed seven-segment information. If you want to analyze such information, or store it, process it or route it, it is more efficient and easier to do if you first convert to a BCD format. Unfortunately, most of the articles that have appeared on this subject in the trade press have presented methods that are expensive, or complicated, or both. Unfortunately, too, the interface problem has aggravated the situation. Thus, the use of calculators, clocks, counters, and A/Ds as number crunchers, real-time clocks, and inexpensive converters has been discouraged. But now, we're pleased to point out, the situation has changed.

It has changed because of our MM74C915—a CMOS seven-segment-to-BCD converter. This device contains, on one chip, all the circuitry you'll need for level shifting, decoding, latching, busing, and even error detection.

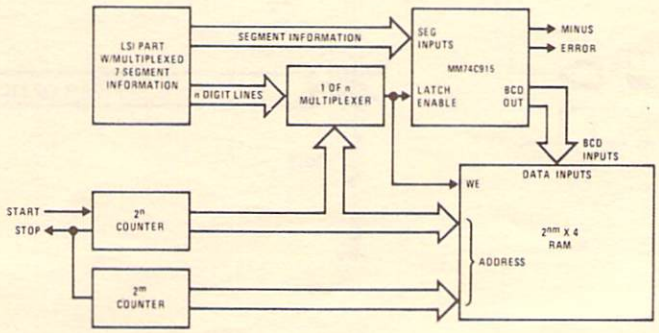
The MM74C915 accepts either positive-true or negative-true inputs. It decodes only legitimate seven-segment characters, allows for variations on the characters one, six, and nine, and gives you an error output when illegitimate characters are present. Its on-chip latch simplifies de-multiplexing a display; the outputs are TTL compatible; and the inputs are MOS compatible without a clamp diode to V_{CC}. And you can use the Tri-State® data outputs for direct data-bus interfacing; there's even a minus-sign output useful in program branching.

With a single MM74C915 you can interface a nine-volt calculator or a watch chip to a five-volt MPU; you can store data in half the memory space, route it with a mux half as wide, process and analyze it twice as efficiently —all without the loss of the price or low parts count of a MOS seven-segment device.

In fact, it's so easy to use and solves so many problems that whenever you think of the seven-segment LSI world, you should also think about the MM74C915.



Multiplex 7-Segment to Straight BCD



Memory Expansion from 7-Segment Outputs

SC/MP Subroutine Supervisor or The Long Arm of P3

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The limited number of registers in the SC/MP makes it a pain in the neck to write large programs with several subroutines and I/O. I finally got tired of setting up pointer registers (my cross assembler does not have the JS macro). Instead, this subroutine supervisor was written which makes programming a lot less boring.

```
                        ;CALL XPPC P3 (P3=SSUP)
                        ;THE FOLLOWING 3 BYTES MUST CONTAIN
                        ;1. FUNCTION CODE
                        ;2. ADDRESS HI
                        ;3. ADDRESS LO
                        ;THE FUNCTION CODE IS AS FOLLOWS:
                        ;  00=RETURN (NO ADDR NEEDED)
                        ;  01=READ (RESULT IN AC)
                        ;  02=WRITE FROM AC
                        ;  03=GOSUB
                        ;THE FOLLOWING ARE INDIRECT ADDR MODES
                        ;I.E. P3 POINTS TO THE ADDR TO BE USED
                        ;P3+0 IS HI,P3+1 IS LO ADDR BYTE
                        ;  04=READ INDIECT
                        ;  05=WRITE INDIRECT
                        ;  06=GOSUB INDIRECT
                        ;THE DEPTH OF NESTING MAY BE CONTINUED
                        ;BUT ONLY FIRST RETURN ADDR IS SAVED
                        ;
                        ;P2-11, -13, AND -14 MUST NOT BE
                        ;DESTROYED BY THE SUBROUTINE
                        ;P2-12, AND -15 ARE ALSO USED.
                        ;TIMING: 341 FOR GOTO, 153 FOR RET.
                        ;+190 MICRCYCLES EXTRA FOR INDIRECT.
                        ;
0200 C2F3    RET:   LD -13(2)       ;RESTORE P3
0202 37             XPAH P3
0203 C2F2           LD -14(2)
0205 33             XPAL P3
0206 C703           LD @3(3)       ;ADJUST FOR RETURN
0208 C2F5           LD -11(2)      ;GET AC
020A 3F             XPPC P3
                        ;*** ENTRY POINT
020B CAF5    SSUP:  ST -11(2)      ;STORE AC
020D C301           LD 1(3)        ;GET FNS WORD
020F 98EF           JZ "RET"
0211 CAF4           ST -12(2)      ;STORE FNS WORD
0213 C302           LD 2(3)        ;SET UP NEW P3
0215 CAF3           ST -13(2)
0217 C303           LD 3(3)        ;H=P2-13
0219 33             XPAL P3        ;L=P2-14
021A CAF2           ST -14(2)      ;SAVE OLD P3
021C C2F3           LD -13(2)
021E 37             XPAH P3
021F CAF3           ST -13(2)
0221 BAF4    STST:  DLD -12(2)
0223 9814           JZ "READ"
0225 BAF4           DLD -12(2)
0227 9816           JZ "WRT"
0229 BAF4           DLD -12(2)
022B 9818           JZ "GTO"
022D C300           LD 0(3)        ;GET SECONDARY ADDR
022F CAF1           ST -15(2)      ;STORE TEMP
0231 C301           LD 1(3)
0233 33             XPAL P3
0234 C2F1           LD -15(2)
0236 37             XPAH P3
0237 90E8           JMP "STST"     ;TEST AGAIN
0239 C300    READ:  LD 0(3)
023B CAF5           ST -11(2)
023D 90C1           JMP "RET"
023F C2F5    WRT:   LD -11(2)
0241 CB00           ST 0(3)
0243 90BB           JMP "RET"
0245 C7FF    GTO:   LD @-1(3)       ;ADJUST P3
0247 C2F5           LD -11(2)
0249 3F             XPPC P3
024A 90BF           JMP "SSUP"

 RET = 0200
SSUP = 020B
STST = 0221
READ = 0239
 WRT = 023F
 GTO = 0245
```

Instead of programming:

```
LD1    "subh"
XPAH   P3
LD1    "subl"
XPAL   P3
XPPC   P3.
```

I now have P3 set once and for all to "SSUP" and program:

```
XPPC   P3
.BYTE  03
.BYTE  "subh"
.BYTE  "subl"
```

which is a saving of 3 bytes. Or better even for a load:

Old Method:

```
LD1    newh
XPAH   P3
LD1    newl
XPAL   P3
LD     0(3)
ST     stack
LD1    oldh
XPAH   P3
LD1    oldl
XPAL   P3
LD     stack
```

New Method:

```
XPPC   P3
.BYTE  01
.BYTE  newh
.BYTE  newl
```

A saving of 14 bytes!

MICRO EDIT

BLOCK TRANSFER FACILITY FOR SC/MP KIT

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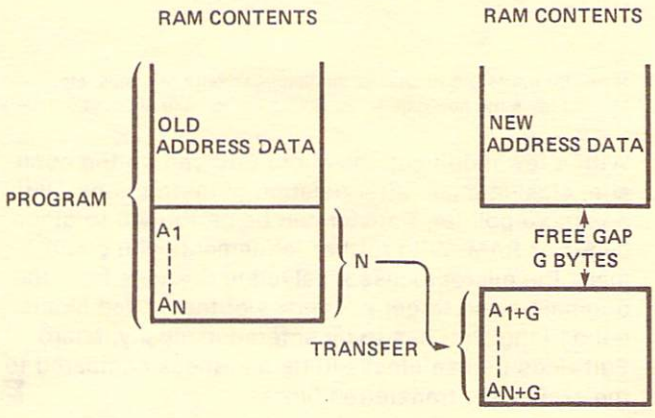
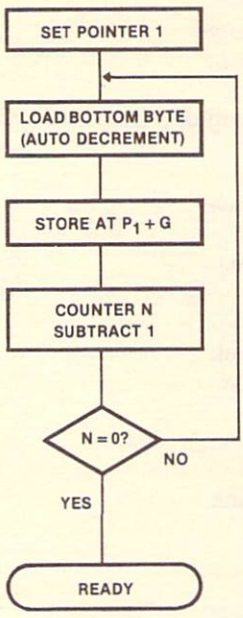
Netherlands

When a program is being developed on a SC/MP Keyboard Kit, insertion of a few extra instructions in the program will include the tedious job of re-entering all following instructions. Block transfer, one of the features of an Editor, does this job for you. Such transfer can be implemented by a nine instruction program, which I named "micro edit". It moves a block of N bytes of RAM contents to a new location, leaving a free gap of G bytes for additional instructions.



FLOW DIAGRAM



User's data: 0Fxx = (P_1): bottom byte original address plus one = A_{N+1}.
nn = number of bytes (N) to be transferred
gg = gap width (G) or transfer distance

PROGRAM ADDRESS	OPCODE	MNEMONIC	COMMENT
0F..	C4	LDI 0F	Set (P_1) = 0Fxx
..	0F		
..	35	XPAH 1	
..	C4	LDI xx	
..	xx		
..	31	XPAL 1	
..	C5	LD a − 1 (1)	Load bottom byte
..	FF		
..	C9	ST gg (1)	Store at new location
..	gg		
..	B8	DLD N	Counter N
..	04		subtract 1
..	9C	JNZ − 8 (0)	Next byte
..	F8		
..	3F	XPPC 3	Back to kitbug if ready
..	nn		Location of counter N

Note: Do not forget to change the displacements of jumps, etc., across the new gap. Micro Edit does not take account of labels.

With a few modifications Micro Edit can do the opposite, closing a gap after deletion of instructions. With one more pointer, transfer can be performed to other pages of RAM. With further refinements you could make the microprocessor calculate G and N from the original — and target addresses of the moved block, but as long as it has to be entered manually, Micro Edit finds its usefulness in its shortness compared to the size of the transferred block.

CMOS 20-PIN OCTAL INTERFACE

A complementary MOS version of the industry-standard 20-pin octal interface family of devices has been developed by National.

The new devices are the first such integrated circuits in commercial production. They incorporate a unique circuit design that allows them to drive high capacitive loads such as one might find when driving a bus and to have a fan-out of 1 when driving standard TTL loads.

First new parts in the CMOS family are the MM54C373/74C373 octal latch and the MM54C374/74C374 D-type flip-flop.

The MM54C373/74C373 is an 8-bit latch. When the latch enable is high, the Q outputs will follow the D inputs. When the latch enable goes low, data at the "D" inputs will be retained at the outputs until the latch enable returns to high again.

The MM54C374/74374 is an 8-bit D-type positive edge-triggered flip-flop. Data at the D inputs is transferred to the Q outputs on the positive-going transition of the clock input.

Both devices feature a wide supply voltage, from 3 to 15 volts; high noise immunity (typically about 45 percent of the supply voltage); low TRI-STATE® output current, about 5 nanoamps; and low power consumption, about 1.0 microwatt at 15 volts. Typical drive (sourcing) current on the devices is about 20 mA per output.

The new CMOS octal interface ICs also feature TRI-STATE outputs, which, in addition to the octal pinouts, make them ideal for microprocessor-bus-oriented systems.

Like their low-power Schottky TTL counterparts — the 54/74LS373 and 54/74LS374, the new CMOS devices are assembled in the new 20-pin dual-in-line package with 0.3-inch centers, which means they only require half the board space of 24-pin packages in a typical PC board layout.

New Maxi-ROM™

Our MM52164 is a static, 65,536-bit (8192 8-bit words) NMOS ROM that features a 450 ns maximum access time and a 24-pin, industry-standard 2316E pin-out.

A single 64K package, in comparison to four 16K packages, obviously lets you pack more memory into a given space. But—somewhat less obviously—at 1/3 the total power dissipation. And in even more subtle ways, a single package saves you money because there are fewer parts to test, fewer programs to inventory, and fewer PC board insertions to perform.

Completely TTL-compatible, the MM52164 operates from a single 5-V supply, is fully decoded, and features programmable Chip Selects that control Tri-State® outputs for easy memory expansion.

The Great Video RAM Myth

National Semiconductor builds and sells both dynamic and static memories. And while we don't like to tell you how you should do things, when we find a more-cost-effective way to do something, we like to pass it on to you.

What we're leading up to is that many users of random-access memories believe, for many applications, static RAMs to be easier to use and less costly than dynamic RAMs. This is a myth that we'd like to lay to rest. And to do so we'll use as an example the CRT terminal—an application for which there appears to be a great resistance to the use of dynamic RAMs.

Now, we've got a part—a 4K dynamic RAM—that works like crazy (275 ns maximum access time, 1 ms refresh) and that's very inexpensive. It's called the MM5280-005, and its price is only about a quarter that of equivalent 4K static RAMs.

To see how this part can save you money, just examine the diagrams shown here. Diagram *A* depicts a CRT terminal. What we've done is to take a SC/MP microprocessor, a DM8678 character generator, and a DP8350 CRT controller, whomped up a video RAM out of eight MM5280-055s (Diagram *B*) hooked them all up to a simple monitor, and—presto!—you've got a CRT terminal. (You can throw in a keyboard, too, if you'd like.)

Note the easy implementation—made possible because the MM5280-055's refresh is automatic in this application, and because only a modest amount of video RAM, control logic (six Schottky packages, Diagram *B*) is required.

But the point of all this is that we've used *dynamic* RAM—not static RAM—to build the terminal's video RAM. We've done so by using eight 4K MM5280-055s, each at a quarter the cost of a 4K static device. This means that even though the system does need a clock, you still reduce video RAM cost by about 50 percent! Mission impossible has become "myth end" accomplished.

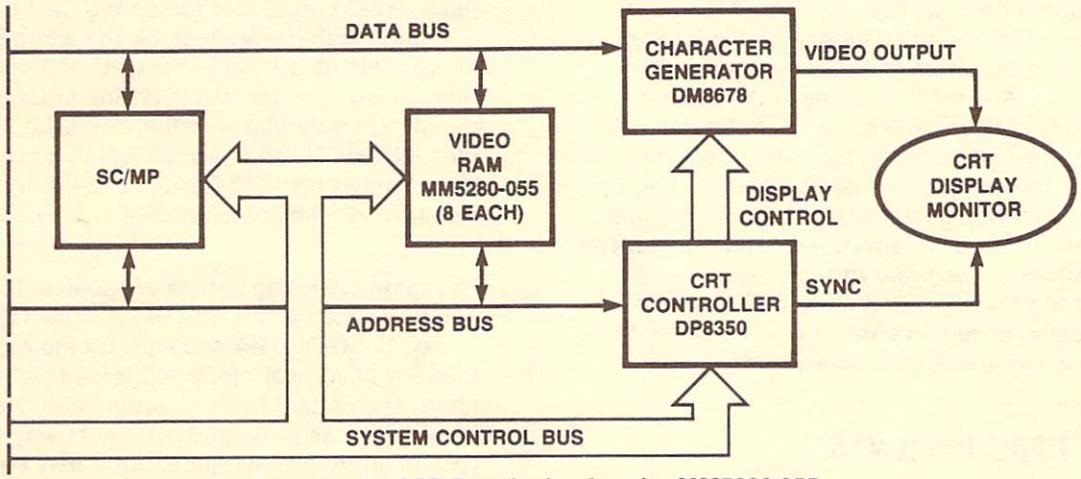


Diagram A. CRT Terminal using the MM5280-055.

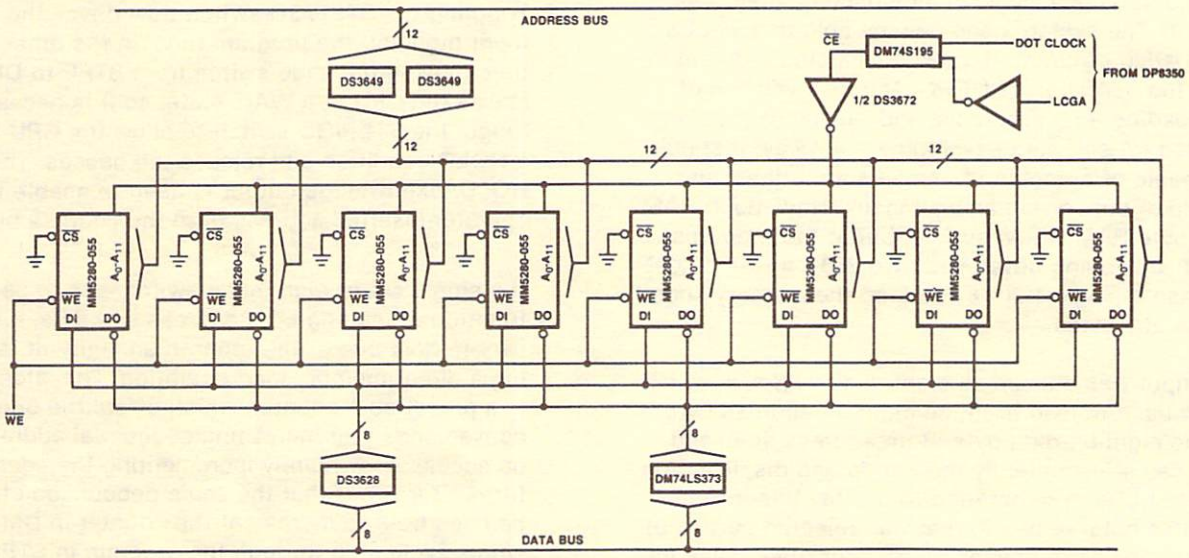


Diagram B. MM5280-055 Video RAM Implementation.

A Review of New Products and Literature from National Semiconductor

MICROTUTOR—An 8080-Based Microprocessor Learning Tool

James C. Gilfert, Ph.D.
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In 1976, I offered a new hardware-oriented course in microcomputers at Ohio University and was gratified by its favorable reception among the students. During the second offering of this course in 1977 the need for a hands-on, in-class tutorial tool became increasingly apparent. It's all well and good to talk about "address out, data back" and so on, but the presentation becomes much more credible if the student is operating his own table-top machine and producing address bits out and observing the data bits back. This article is the result of efforts to assemble an absolute minimum 8080-based system that would allow for direct memory loading, single-step or continuous execution, and constant monitoring of data bus and address bus.

The reader is perhaps tempted to ask, "Why an 8080-based system?" There are other CPUs with more versatile instruction sets, true. But the 8080 is currently the CPU that the practicing engineer is most likely to encounter, it has probably the most extensive software library, and it offers perhaps the easiest instruction set to learn. Again, we might be tempted to argue that several support chips are required for the 8080. For more complex systems, this is true, but at the minimum level, only a CMOS clock is required; no status latch, no bus interface, no control logic. The slight nuisances of the triple-voltage supply (+12V, +5V, −5V) and the high-level clock requirements were considered acceptable in view of the below-$15 price range where the 8080 is now selling.

SYSTEM REQUIREMENTS

What comprises a viable minimum-component learning tool? The system need only be able to accept a hand-loaded program of a few dozen steps to demonstrate the operation of a CPU. The user will tire of hand-loading long programs, and the microtutor is not intended for software development anyway. It should be capable of branching to small subroutines, and capable of supporting a small stack. How much RAM? A 128-byte RAM would suffice, but at the time this system was being developed, two 256 × 4 RAMs cost less than a single 128 × 8 RAM, so the memory ended up with 256 bytes.

User input was chosen as eight slide switches which can be used to load both the eight-bit address byte and the eight-bit data byte. Both address lines and data lines are constantly monitored and displayed on discrete LEDs. A temptation to display this information in an octal or hex format was rejected partly out of cost considerations, and partly because it was felt that a fuller appreciation of the processes would be gained at the individual bit level.

Three operating modes were desired: DMA, which frees the CPU from the address bus and data bus, thereby allowing the user to load in or modify a program from the slide switches. STEP, to allow single-cycle execution of a program. This mode is invaluable from the teaching standpoint, because each cycle of a multi-cycle instruction such as memory or stack reference, is vividly documented by the LEDs as execution proceeds. Finally, of course, a RUN mode is required to allow the program to be executed without interruption.

HARDWARE CONSIDERATIONS

The CPU communicates only with its RAM (see Figure 1), therefore, only memory read and memory write control signals are required. The 2112 RAM was chosen because it is automatically in read whenever its chip enable is activated, unless R/$\overline{W}$ is also driven low. This RAM needs only to be disabled during the status output time of the CPU to avoid a conflict of two drives on the data bus. This is readily achieved by driving the RAM's $\overline{CE}$ input with SYNC from the 8080.

Single-cycle stepping requires a flip-flop whose output drives the CPU READY input low at the rising edge of each SYNC pulse. This forces the CPU into a WAIT condition with the address on the address bus and the appropriate data from either CPU or RAM on the data bus. These data are visible on the LEDs. When the operator is satisfied with the displayed data, he toggles a STEP/GO slide switch which clocks the flip-flop and restores the CPU READY input to a running condition through the completion of that cycle.

The three operating modes are selected by a three-position slide switch. The STEP mode is deliberately placed between DMA and RUN on the mode switch so that any change of mode will leave the CPU in a WAIT state. Thus after loading a program in DMA, the mode control passes through STEP on its way to RUN. The CPU is left in a WAIT state, but it may be RESET while in WAIT. This restores the program counter to zero. Toggling the STEP/GO switch now drives the READY input high and the program runs. In the other direction, moving the slide switch from STEP to DMA also leaves the CPU in a WAIT state, so it is necessary to toggle the STEP/GO switch to allow the CPU to enter a HOLD condition and release the busses. The CPU's HOLDAcknowledge output is used to enable the operator-inserted address onto the address bus.

If a single set of eight slide switches is to serve the function of loading both address and data, it is necessary to hold one or the other in an eight-bit latch during a direct memory load operation. The latch chosen is a presettable counter, which offers the operating convenience that increasing sequential addresses may be accessed by merely incrementing the counter. It further turns out that the same debounced step can be used both to increment the counter in DMA, and to single-cycle step through the program in STEP. Similarly, the same RESET button resets both the address counter and the CPU.

CMOS chips were chosen wherever feasible. The LED drivers are 4049s because they add only a few pF load to the lines they display. A 4049 operating on + 12V was used as the RC clock and high-level driver. The RC constants suggested provide a clock frequency around 300 kHz. The presettable counter is a cascaded pair of 4516s. The external address and data are tri-stated to their busses by TTL-type 81LS95s, chosen because they handle the eight-bit word in a single package. A 4013 dual D flip-flop implements the single-cycle step and also debounces the STEP/GO switch. Because the 8080 requires at least 3.3V as its logic ONE input, 10K pull-up resistors were added to the data bus.

The original version was assembled using solder-tail sockets and a wiring pencil for all signal lines. If this construction technique is used, all connections should be verified with an ohmmeter as they are made. Alternate construction methods may be preferable, depending on your own experience. The system was assembled on perfboard, then mounted on a 5 × 7 × 3 aluminum chassis. The chassis provides mounting for the slide switches, and the power supply is mounted inside. Power requirements are: + 12V at 60 mA, + 5V at 250 mA, and − 5V at 1 mA.

If you'd like to check your clock speed, load the following program:

Addr	Data	Mnemonic	Clock Cycles
00	21	LXI H	10
01	FF	FF	
02	FF	FF	
03	2B	DCX H	5
04	7C	MOV A,H	5
05	A7	ANA A	4
06	C2	JNZ	10
07	03	03	
08	00	00	
09	76	HLT	7

After initializing register pair HL with FFFF ($= 65{,}536_{10}$), the program enters a loop which decrements the register pair one count for each loop. The loop is exited when (HL) = 00FF ($= 256_{10}$), i.e., after 65,280 loops. Since each loop requires 29 clock cycles, the number of clock cycles in the loop is 1,893,120. If your clock runs at 300 kHz, as mine does, the lamps will stop after about six seconds.

Most of the ideas incorporated in this could be readily extended to implementation of minimum systems with other CPUs. The major nuisance with this system is the slide switch data/address entry, and you may wish to substitute a hex keypad and 74C922 encoder.

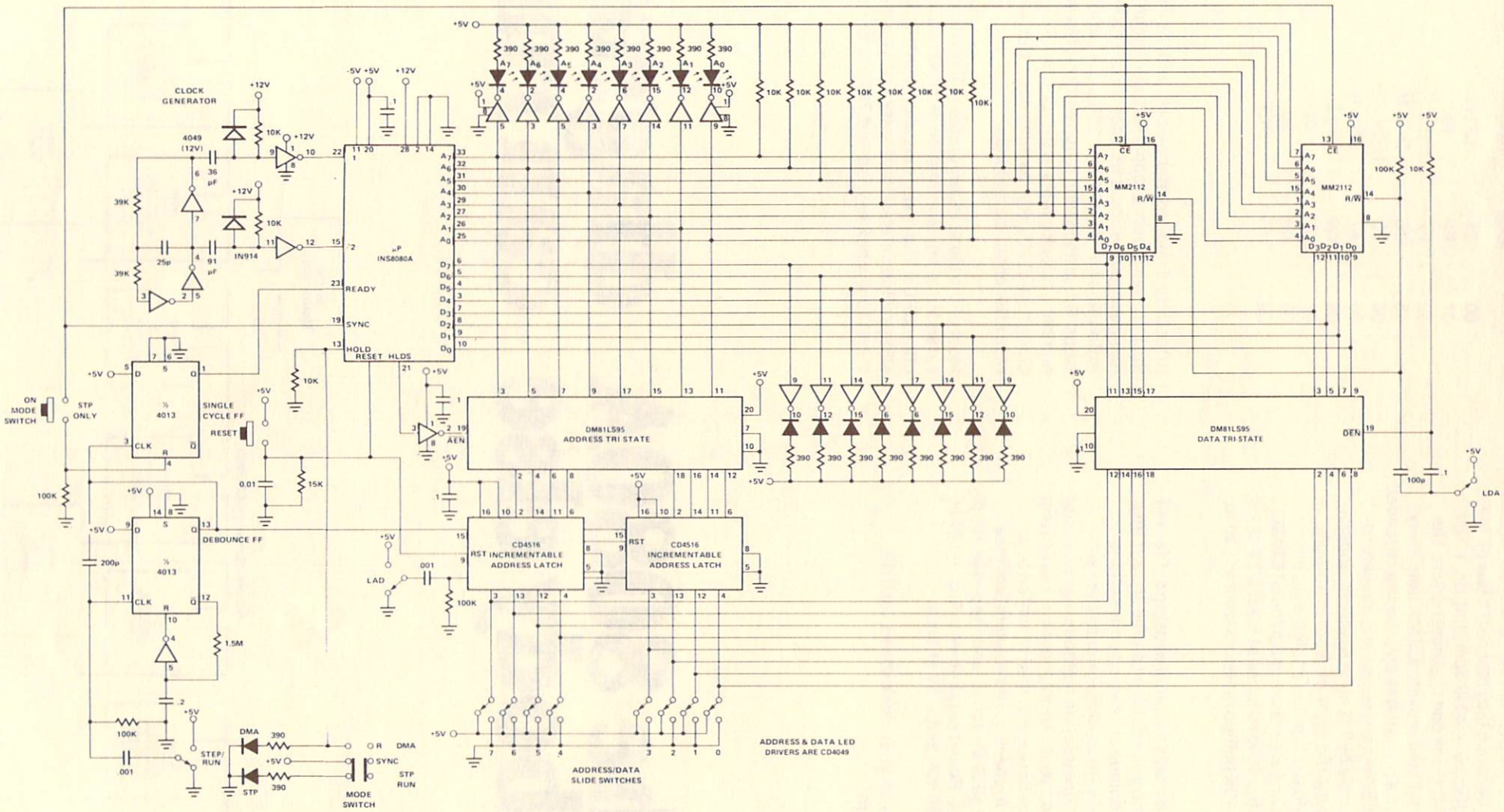


FIGURE 1: MICROTUTOR LEARNING TOOL

the Bit • Bucket

Dear Georgia:
After getting NIBL up and running it became evident that if I wished to be able to store programs, a tape reader relay was required as shown on p. 2-11 of the LCDS Users manual. Being lazy I accomplished this as shown below (Figure 1).
There is plenty of room to mount the SSR (Solid State Relay) in the area behind the tape punch along with the plug of your choice. The installation is easy and will take about 20 minutes. The switch when closed will revert the TTY to its original condition.
Yours truly,
R.W. Henderson, P.Eng.
Instructor, Electrical Dept.
Northern Alberta Institute of Technology
11762 - 106 Street
Edmonton, Alberta, Canada T5G 2R1

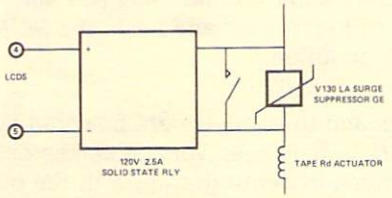


FIGURE 1: READER CONTROL USING SOLID STATE RELAY

Dear COMPUTE:
Please send me the SC/MP program NIBL number SL0043A. A check of $15 is enclosed. Is it possible to obtain a listing of the line-by-line resident assembler presented in COMPUTE, Vol. 3, No. 6, June 1977? I do not have a LCDS but a home-brew system. However, I think I will be able to modify the software to suit my system.
Sincerely yours
Sten Nyberg
Nybykroken 1
163 70 Spanga, Sweden

The line-by-line assembler, SUPAK, is a proprietary product and listings of the source are not available. It can be ordered in ROM from your local distributor by specifying ISP-8F/111. The cost is $150. It can be plugged into the blank ROM/PROM card (ISP-8B/004B).

Gentlemen:
Enjoyed Mr. Leon Minton's article on using a SC/MP as a ASCII to Baudot Converter in Vol. 3, No. 1. Do you know of a source of preprogrammed MM5204Q's or programming tapes?
Stuart E. Neblett
PG&E Communications
1970 Industrial Way
Belmont, CA 94002

Some National distributors will program PROMs for you, if they are purchased from them. In the Bay Area Hamilton-Avnet has a microprocessor lab and may be able to perform the services you wish. Contact them at (415) 961-7000. Any other users, know of alternatives? Please write and let us know.

Dear Georgia:

I am in the process of building a system around the SC/MP chip.
However, most of the programs I am interested in, are written in PACE BASIC, (for example SL0048A Biorhythm).
For beginners to SC/MP may I suggest to COMPUTE readers "A Guide to SC/MP Programming"by Kemitron Electronics, available from Kemitron Electronics, 65 Warren Rise, Frimley, Camberley, Surrey, England.
Finally, there's an amateur computer club in Britain that might be of interest to your European readers. They should contact Mike Lord, Amateur Computer Club, 7 Dordells, Basildon, Essex, England.
Many Thanks,

Mel Pearce
21 Hall Meadow
Wedges Mills
Cannock, Staffs WS11 1TB
England

Dear Georgia:

I received the SC/MP information you sent, and it answered most of my questions. You, or whomever is responsible for the format, etc., of COMPUTE are to be congratulated. It is an excellent job.
However, I do have one left-over question. Is the SC/MP kit available with the SC/MP-II, or must the -II be purchased separately as a retrofit kit?
Thank you

James C. Matthews
2028 Merrily Drive
Montgomery, AL 36111

The answer is yes. The SC/MP-II retrofit kit must be purchased separately. (Order No. ISP-8K/205 — $18.50). For changes to the ROM-to-reflex timing difference between SC/MP-I and SC/MP-II, see COMPUTE, Vol. 3, No. 5, p. 19.

Dear Sirs:

I have recently learned that Hal Chamberlins' IMP-16 design has been continued in your magazine COMPUTE (after the Computer Hobbyist died!) I understand that Part 3 was published in the November 1976 issue. Could you send me a copy, please?

Carolyn Benson
8130 Pt. Douglas Dr. S.
Cottage Grove, MN 55016

SC/MP Control Panel

by Ronald G. Parsons
9001 Laurel Grove Drive
Austin, Texas 78758

The circuit described below is designed to provide more information and control over running programs than is possible using the base SC/MP Kit and Keyboard Kit. Features include:

- Data or address bus display in hex.
- Automatic (variable speed) and manual single-stepping in either single cycle or single instruction mode.
- Sense switch for Sense A input.
- Reset switch.
- Display of R-, I-, D- and H-flags.
- Display of Flag 1 and Flag 2 outputs.
- Bus access switch (puts SC/MP bus lines in TRI-STATE).
- Brightness control for displays.

The letter pairs, e.g., (DV), indicate the ICs involved on the schematic (Figure 1). Figure 2 shows the component layout.

The circuit is wire-wrapped on a board with 44-pin edge connectors. The SC/MP can be run with or without the Control Panel board in its socket. The switches shown on the schematic are on the panel near the edge connector. The display drivers (DV thru DY) can be either 7447s or 8673s. The latter give correct hex displays for A-F while the former give unique (but strange) displays for A-F.

The four-digit data/address display is set by a flip-flop (DZ) to display either a four-digit address or a two-digit data byte with the upper two digits blanked. The address and data bus contents are latched (CU thru CZ) during the NADS, NRDS or NWDS strobes so that both busses are available for display while the processor is stopped (CONT or NHOLD Low). The R-, I-, R-and H-flags are also latched (CT). The multivibrator (DT) controls the intensity of the bus displays.

The address and data busses are buffered through CMOS drivers (BV thru BZ) so the busses are loaded as little as possible.

The Single-Step and Halt controller (AU and AZ), combine the circuits of Figures 2-7 and 2-8 in the SC/MP Technical Description.

The displays and their drivers are powered by separate 5V regulators to help keep voltage spikes caused by display changes from interferring with the other ICs on the card.

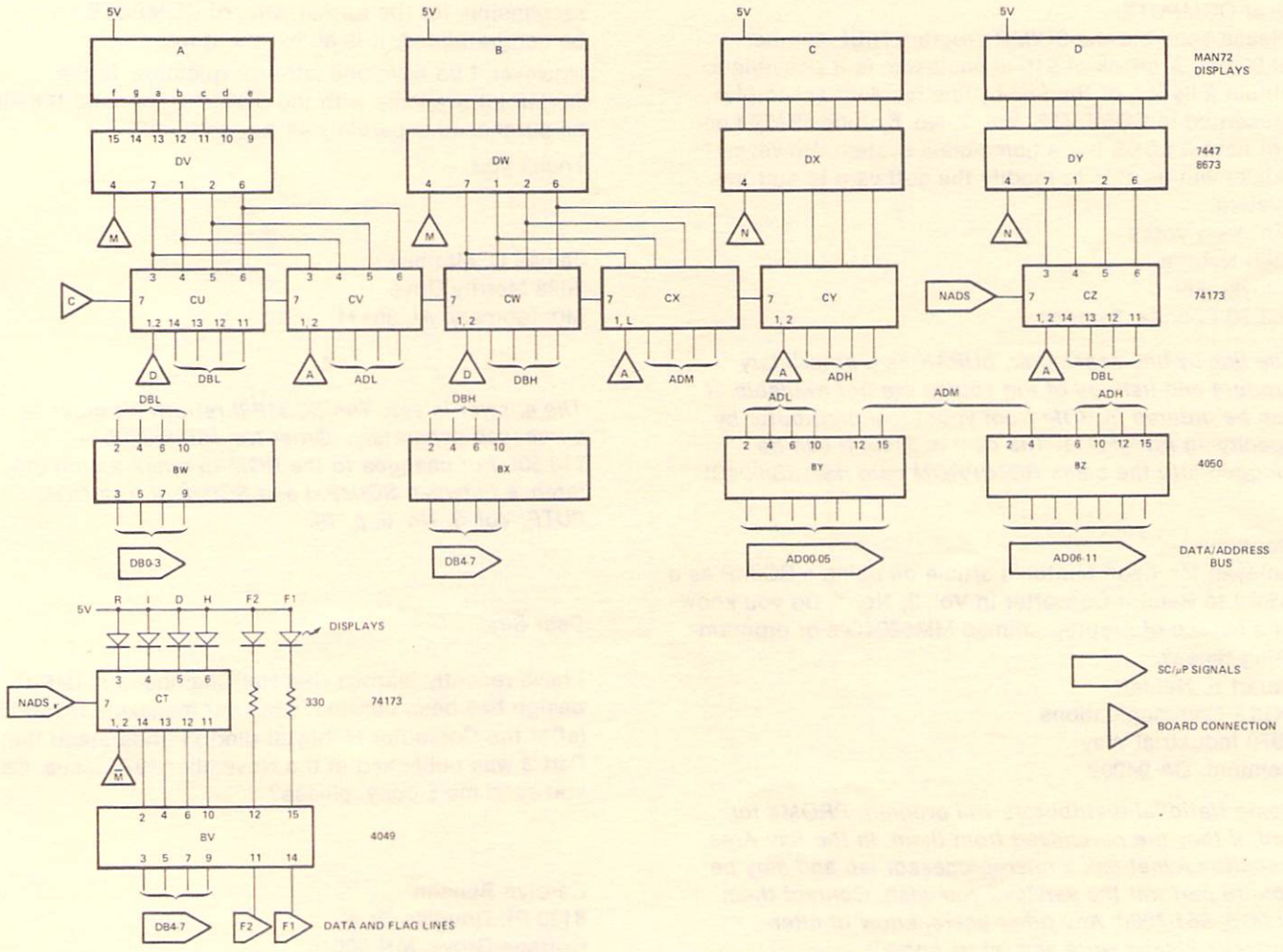


Figure 1. Control Panel Circuits

Multiprocessing with SC/MP

National Semiconductor
Application Note 197
Keith Winter
November 1977

ABSTRACT

This application note presents a brief analysis of the multiprocessing capabilities and characteristics of the SC/MP 8-bit microprocessor based on measured data.

INTRODUCTION

One of the outstanding features of the SC/MP microprocessor (ISP-8A/500 or INS8060) is the built-in bus allocation logic for both multiprocessor and Direct Memory Access (DMA) applications. All the necessary control logic and timing signal generation is provided on-chip. In a multiprocessor configuration, "daisy-chaining" automatically assigns the priorities of each processor, thus eliminating the need for external priority generation logic.

However, some questions concerning the advantages or disadvantages of multiprocessing arise: What percentage increase in throughput can be expected? At what point does the bus become overloaded? These and other questions will be answered in this application note.

TEST CIRCUIT IMPLEMENTATION

Hardware

To acquire the data to answer these questions, a test board was constructed which allowed from one to four SC/MPs to be connected to a common bus in a "daisy-chain" prioritized configuration (see figure 1). In this manner, SC/MP #1 has the highest priority, SC/MP #2 has second, etc. To maintain a record of each processor's relative throughput, a counter circuit was added to Flag 2 of each of the four SC/MPs. This enabled each processor to clock the counter with a pulse flag instruction sequence. A Teletype® (TTY) interface was added to Flag 0 of SC/MP #1 so the circuit could output the test sequence results.

A simple method was used to determine which SC/MP would perform all data collection and display duties of the system. The Sense-B port for SC/MP #1 was tied to V_{CC} and the Sense-B ports of all others were grounded. The Sense-B port of each SC/MP was then examined to determine which one (in this case SC/MP #1) would read the data out of the counters and display that data on the TTY printer. Since all processors shared the same instruction memory, those that were not to print the data simply branched back to the initial wait loop to await the next timing pulse. When the SC/MP doing the printing finished, it too branched back to the wait loop.

® Registered trademark of the Teletype Corporation

Software

Two test programs were written: a worst case and a typical. In the worst case program, instructions were chosen which require a high percentage of bus time (i.e., CAS, LDE, XAE, SIO). These instructions and a pulse flag instruction sequence formed a timing loop. This loop was executed for a preset time duration, in this case 20 ms. At the end of the timing period, the contents of each counter were displayed. In the typical application program, a more normal distribution of instructions was chosen which included those which allow more free time on the bus (i.e., ILD, DLD, LD, ST). These instructions replaced the worst case instructions in the timing loop and the test sequence was repeated.

The test sequence consisted of running the test programs with one SC/MP, as a control, then successively adding more SC/MPs, rerunning the programs and recording the counter contents. Since the contents of the counters indicate the amount of work accomplished during the timing period, it is also an indication of individual processor throughput. The summation of the work done by all SC/MPs yields a value indicative of system throughput.

The assembly listings of the two test programs are shown in the Appendix. For brevity, the data collection and TTY output routines are not shown.

DA-B20M117/Printed in U.S.A.

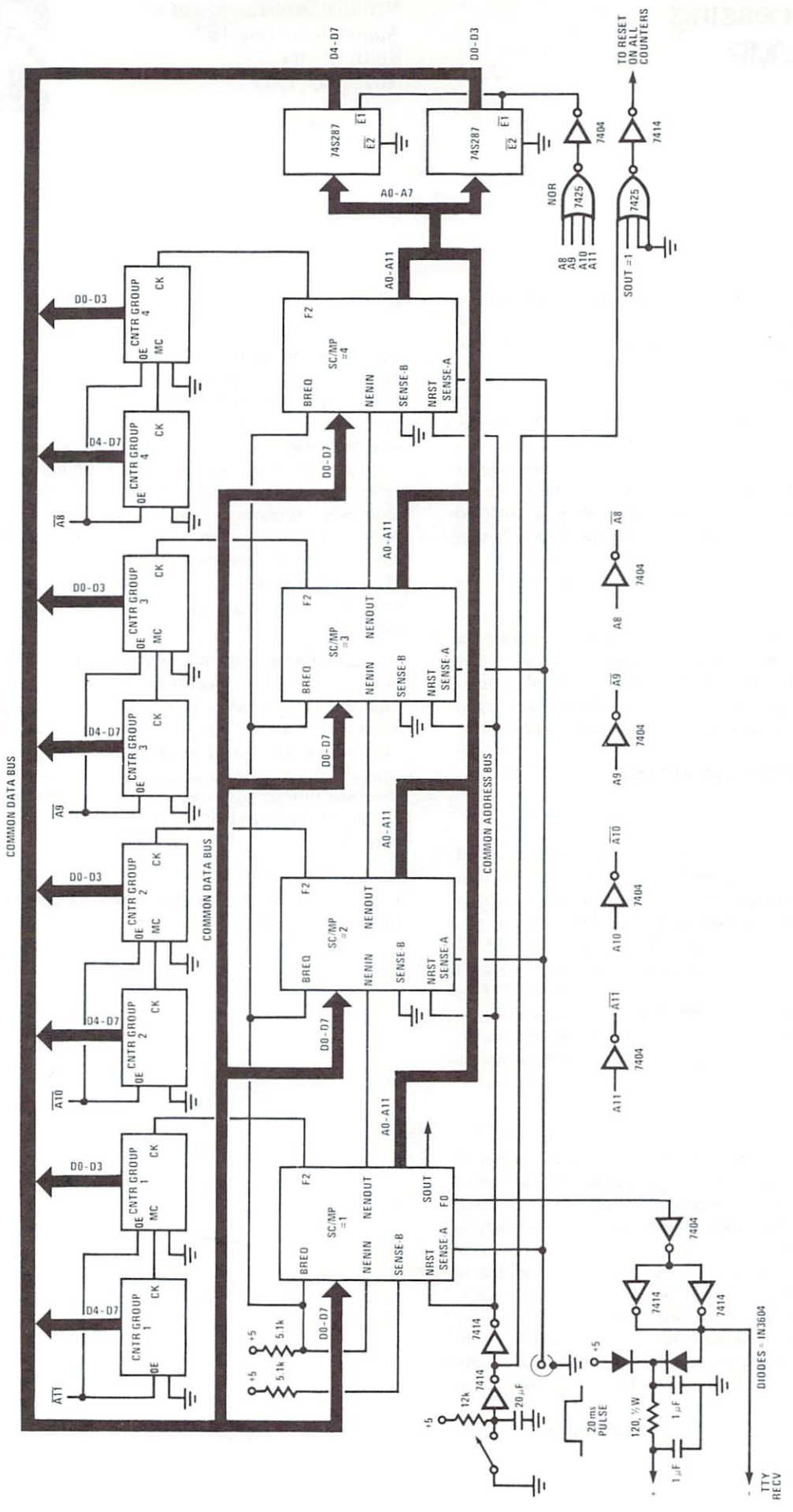


Figure 1. Four SC/MPs in "Daisy Chain" Configuration

RESULTS

From the data obtained for each case, a curve can be drawn which depicts the percentage of throughput increase as additional SC/MPs are added (see figure 2). Also, from the same data, a plot of bus access can be drawn (see figure 3).

From figure 2, note that as more processors are added the percentage of throughput increase decreases, and if the curve is extrapolated past four SC/MPs it is apparent that it will eventually flatten out as the bus becomes saturated. From the worst case plot, it can be seen that the curve has already flattened out between three and four SC/MPs and it appears that there will be no further significant increase in throughput. However, the typical plot shows that there will be an increase in throughput at least up to the addition of a fifth processor on the bus. The actual measured results for the typical applications program showed that with one SC/MP referenced as 100% throughput, two SC/MPs yield a 93% increase in throughput, three SC/MPs yield a 140% increase, and four SC/MPs yield a 158% increase. The incremental throughput is 93% for the second SC/MP, 47% for the third, and 18% for the fourth. From these values it appears that to gain the greatest increase in throughput from the same system resources, the maximum number of SC/MPs to put on the bus would be four, with two giving the highest overall performance increase per added processor.

Figure 3 illustrates what percentage of the available bus time was used by each SC/MP. As the priority of each processor goes down, the amount of bus time available to it also goes down. When four SC/MPs are on the bus, the one with the lowest priority, in this case number four, is receiving only about 19% of the bus, whereas the one with the highest priority is on the bus about 29% of the time. This gives an indication of the automatic prioritizing done when multiple SC/MPs are connected in the "daisy-chain" configuration.

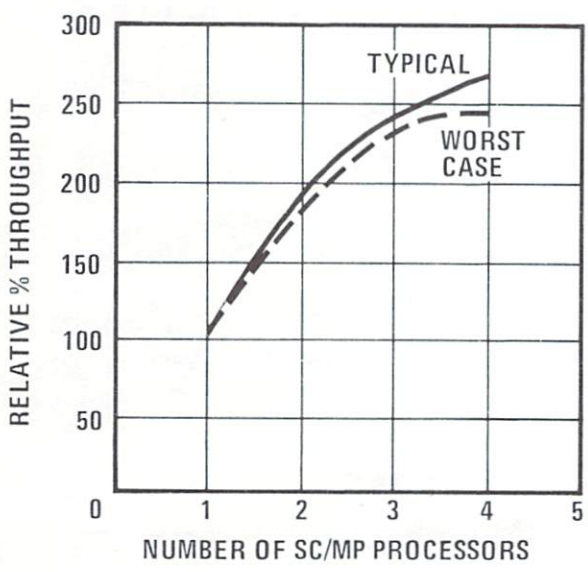


Figure 2. Percent Throughput vs Number of Processors

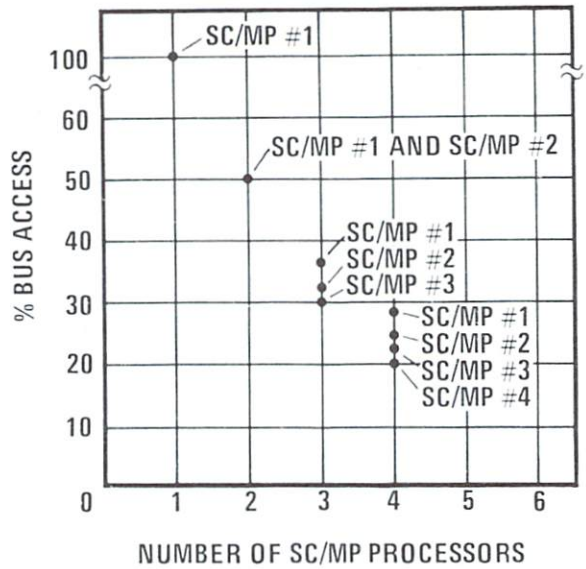


Figure 3. Percent Bus Access vs Number of Processors

SUMMARY

This application note is the first in a series of papers on the subject of multiprocessor applications of the SC/MP microprocessor. The data presented should aid the SC/MP user in the determination of the number of processors to place on a single bus with shared resources. The type of task or tasks to be performed is a major factor in the determination of both the number of processors required and the circuit configuration to be used. Future application notes will cover these considerations.

```
                        .TITLE  MULTIS,  'WORST CASE TEST'

                ; Pointer and Flag definitions

        0001    P1      =       1
        0002    P2      =       2
        0003    P3      =       3
        0001    F0      =       1
        0002    F1      =       2
        0004    F2      =       4

0000    08              NOP
                CLR:
0001    C401            LDI     1       ;clear counters by pulsing the
0003    01              XAE             ; SOUT port
0004    19              SIO
0005    19              SIO
                WAIT:
0006    06              CSA             ;check SENSE-A for start
0007    D410            ANI     010
0009    98FB            JZ      WAIT    ;continue scanning
                PULSE:
000B    06              CSA             ;check SENSE-A port for end of
000C    D410            ANI     010     ; timing period
000E    980C            JZ      PRINT   ;print counter contents

0010    40              LDE             ;these instructions require a
0011    01              XAE             ; high percentage of bus time
0012    06              CSA             ; per instruction cycle

0013    06              CSA
0014    DC04            ORI     F2      ;pulse flag 2 to clock counter
0016    07              CAS
0017    D4FB            ANI     %F2
0019    07              CAS
001A    90EF            JMP     PULSE   ;continue looping
                PRINT:
001C    06              CSA             ;read SENSE-B port
001D    D420            ANI     020
001F    98E5            JZ      WAIT    ;if zero, don't print.  This
                                        ; determines which SC/MP will
                                        ; print the data.

                ; Print routines follow this

                PHEX:
                ;       .
                ;       .
                ;       .
```

```
                        .TITLE  MULTIS, 'TYPICAL DISTRIBUTION TEST'

                ; Pointer and Flag definitions

        0001    P1      =       1
        0002    P2      =       2
        0003    P3      =       3
        0001    F0      =       1
        0002    F1      =       2
        0004    F2      =       4

0000    08              NOP
                CLR:
0001    C401            LDI     1       ;clear counters by pulsing the
0003    01              XAE             ; SOUT port
0004    19              SIO
0005    19              SIO
                WAIT:
0006    06              CSA             ;check SENSE-A for start
0007    D410            ANI     010
0009    98FB            JZ      WAIT    ;continue scanning
                PULSE:
000B    06              CSA             ;check SENSE-A port for end of
000C    D410            ANI     010     ; timing period
000E    980F            JZ      PRINT   ;print counter contents

0010    C100            LD      (P1)    ;these instructions release
0012    C900            ST      (P1)    ; the bus for a significant
0014    A900            ILD     (P1)    ; period of time.

0016    06              CSA
0017    DC04            ORI     F2      ;pulse flag 2 to clock counter
0019    07              CAS
001A    D4FB            ANI     %F2
001C    07              CAS
001D    90EC            JMP     PULSE   ;continue looping
                PRINT:
001F    06              CSA             ;read SENSE-B port
0020    D420            ANI     020
0022    98E2            JZ      WAIT    ;if zero, don't print.  This
                                        ; determines which SC/MP will
                                        ; print the data.

                ; Print routines follow this

                PHEX:
                ;       .
                ;       .
                ;       .
```

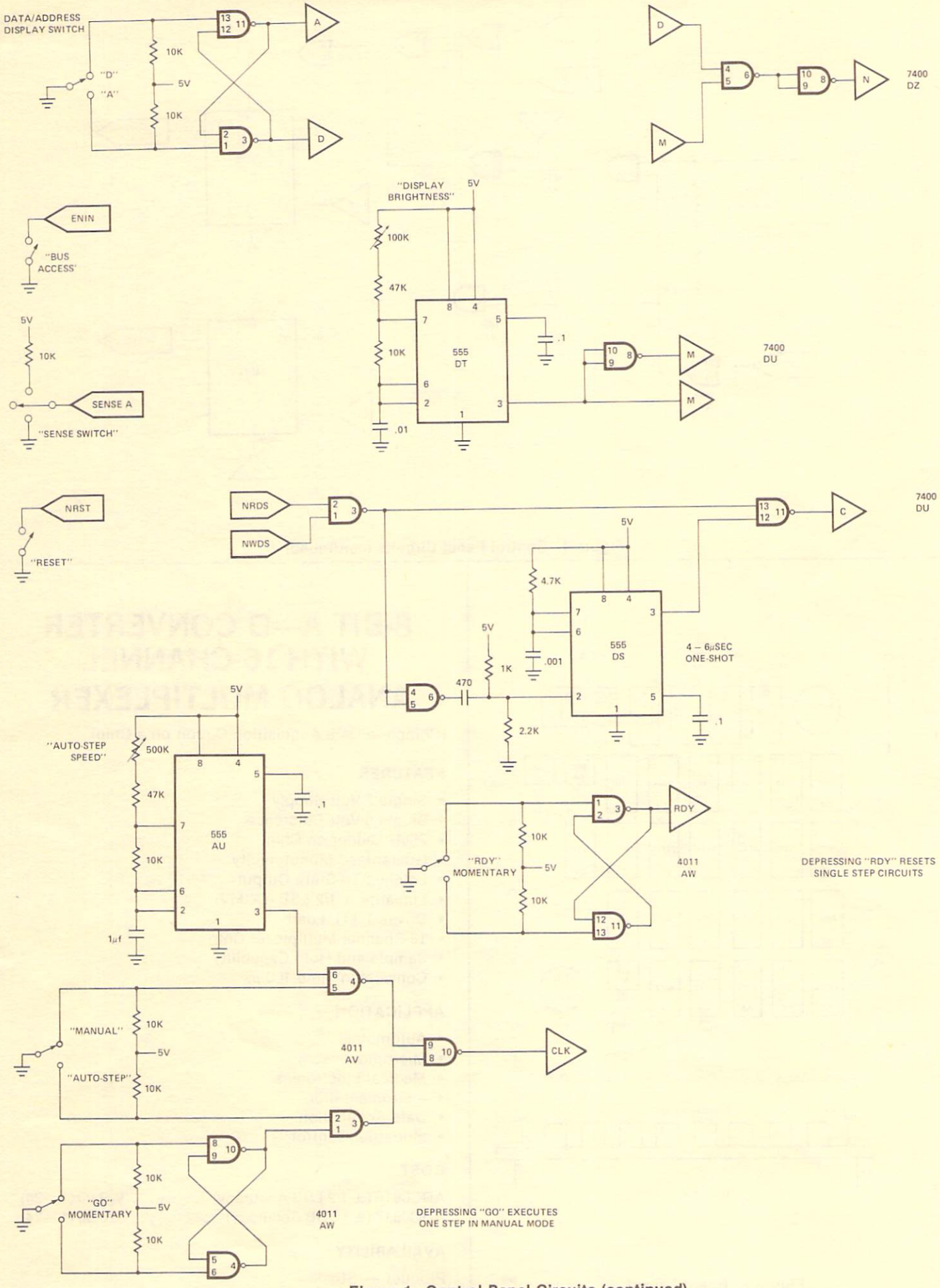


Figure 1. Control Panel Circuits (continued)

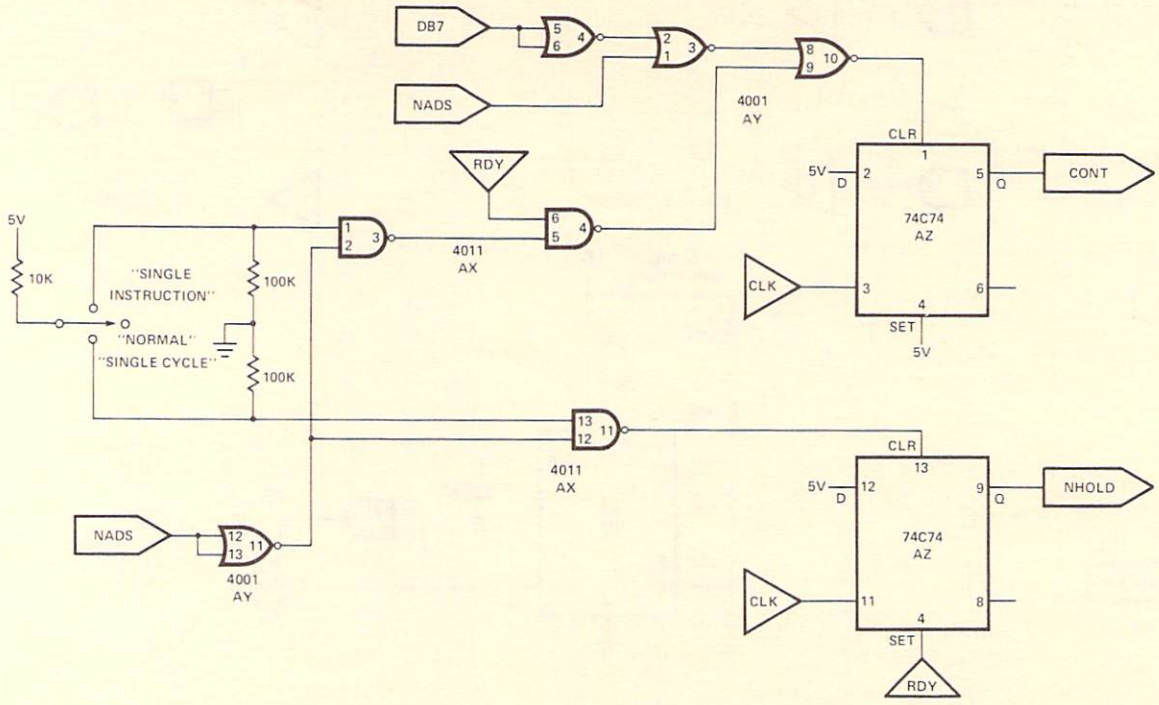


Figure 1. Control Panel Circuits (continued)

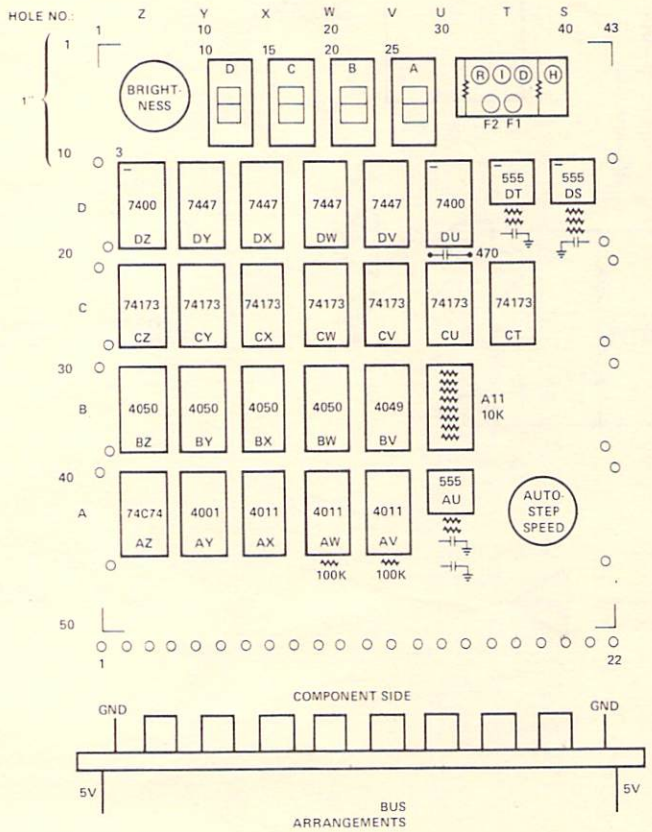


Figure 2. Board Layout

8-BIT A—D CONVERTER WITH 16-CHANNEL ANALOG MULTIPLEXER

(Complete Data Acquisition Circuit on a Chip)

FEATURES

- Single 5-Volt Supply
- Single 5-Volt Reference
- 256R Ladder on Chip
- Guaranteed Monotonicity
- Latched Tri-State Output
- Linearity ± 1/2 LSB (COMV)
- Drives 1 TTL Load
- 16-Channel Multiplexer Chip
- Sample and Hold Capability
- Conversion Time 100 μs

APPLICATION

- Automotive
- Microprocessors
- Medical Electronics
- Instrumentation
- Data Acquisition
- Industrial Control

COST

ADC0816 (± 1/2 LSB Accuracy) . . . . . $29.00 (1—24)
ADC0817 (± 1 LSB Accuracy) . . . . . $26.80 (1—24)

AVAILABILITY

Product — Stock
Data Sheets — Printed, call Marketing Services.

Reverse Polish

by Lawrence J. Stempnik
Senior Project Engineer
Schiller Industries, Inc.
7111 E. Eleven Mile Rd.
Warren, MI 48090

REVERSE POLISH PAPER TAPE LOADER

The Reverse Polish Notation developed by Jan Lukasiewicz results in calculator simplifications due to the parenthesis-free notation. In a similar manner, a Reverse Polish Paper Tape Loader can be written with just seven opcodes. This program will load up to 230 memory locations in the standard KITBUG configuration from a punched paper tape.

This RPPTLD program is very helpful in loading debugged programs into SC/MP from teletypes. A forward loading tape program can be used but it requires three times more typing to load it manually and it takes up more storage locations.

To use the program, a special paper tape must be prepared, either manually or with a microprocessor. Each line consists of two consecutive pairs of hex digits plus a carriage return or line feed, but not both. The tape is then punched with each four character line in reverse sequence. Punch the last four digits to be stored first, and continue until reaching the first four digits to be stored.

This RPPTLD program uses the GHEX subroutine in KITBUG. The same rules as MODIFY apply when entering more or less than four digits per line. If more than four digits are entered on one line, only the last four are used. A CR without numbers results in 00 being stored in two consecutive memory locations. If one to three digits are entered before CR, GHEX will supply leading zeros to produce four digits. For convenience in handling the paper tape and reader, enter 20 leading zeros on the first and last line of the tape.

Pointer P1 must be set to 00DF for GHEX. Pointer P2 points to one plus the last storage location (end of program to be stored). To use the program, type in the seven opcodes plus the three pointer registers using the MODIFY command. Load the paper tape in the reader and position to start of first line of data, type G, return, and turn tape reader on. After tape is loaded, hit RESET and return control to KITBUG.

```
02E7  35  XPAH   P1   H(GHEX)
02E8  37  XPAH   P3   HI = 00
02E9  31  XPAL   P1   L(GHEX) – 1
02EA  33  XPAL   P3 = 00DF = GHEX – 1
02EB  3F  XPPC   P3   GET TAPE INPUT
02EC  90  JMP    REPEAT TO END OF TAPE
02ED  FD  P0-3
```

REVERSE POLISH PAPER TAPE PUNCH

This SC/MP program is used to prepare tapes to be loaded into SC/MP using the RPPTLD program. It prints (punches) four consecutive hex characters per line from storage with the lines in reverse sequence. Each line ends with CR but does not use line feed.

KITBUG subroutines used are PHEX2 for printing (punching) the hex characters and PUTC for the CR. To use the program, set P0 and P2 to 02D7 and set P1 to 1 plus the last line of the stored data or program. Turn on the paper tape punch just before running the program. The paper tape will be punched as the teletype prints the lines. About 208 bytes can be punched using memory locations 02CF through 0200.

```
02D0  XX  XX          USED BY SUBS
02D1  XX  XX          USED BY SUBS
02D2  XX  XX          USED BY SUBS
02D3  XX  XX          AD HI
02D4  XX  XX          AD LO
02D5  XX  XX          USED BY SUBS
02D6  XX  XX          USED BY SUBS
02D7  C4  LDI         REV POL PT PCH
02D8  01  HEX = DECIMAL + 1
02D9  37  XPAH   P3   HI = 01
02DA  C4  LDI         L(PHEX2) – 1
02DB  43  HEX = DECIMAL + 67
02DC  33  XPAL        P3 = 0143 = PHEX2 – 1
02DD  C5  @LD         MOVE PUNCH POINTER
02DE  FE  P1 – 2
02DF  3F  XPPC   P3   PRT HI BYTE
02E0  C4  LDI
02E1  43  HEX = DECIMAL + 67
02E2  33  XPAL        P3 = 0143 = PHEX2 – 1
02E3  C1  LD
02E4  01  P1 + 1
02E5  3F  XPPC   P3   PRT LO BYTE
02E6  C4  LDI
02E7  C4  HEX = DECIMAL – 60
02E8  33  XPAL        P3 = 01C4 = PUTC – 1
02E9  C4  LDI
02EA  0D  HEX = DECIMAL + 13
02EB  3F  XPPC   P3   PRT CR
02EC  90  JMP         REPEAT TO START PROG
02ED  E9  P0 – 23
```

Future Memory Development

by Thomas Klein, NSC

ABSTRACT: Semiconductor integrated circuit based memory devices became the dominant Random Access Memory technology in less than 8 years. They were able to achieve this because their batch manufacturing process allowed a very rapid reduction of cost per bit of storage through technological changes to increase batch density. Continued progress in density improvement at essentially unchanged rates is still feasible. It will, however, require major changes in manufacturing, device and material technology.

Since the beginning of the 70's, semiconductor integrated circuits used as digital storage elements have become a very significant factor in the total spectrum of information storage technology. They became the dominant technology for random access memories and are beginning to make inroads into the slower serial access memory market, presently dominated by magnetic discs and drums.

The ability of integrated circuit technology to continue to offer digital data storage at very rapidly decreasing cost per bit of storage is a consequence of the batch manufacturing process. It allows introductions of new products which are cost effective even at very low manufacturing efficiency level, obtain very steep cost reduction during product life by rapid increase of manufacturing efficiency and continue to stay on the steep cost reduction curve by going to a higher level of integration when cost improvements through improved manufacturing efficiencies are starting to flatten out.

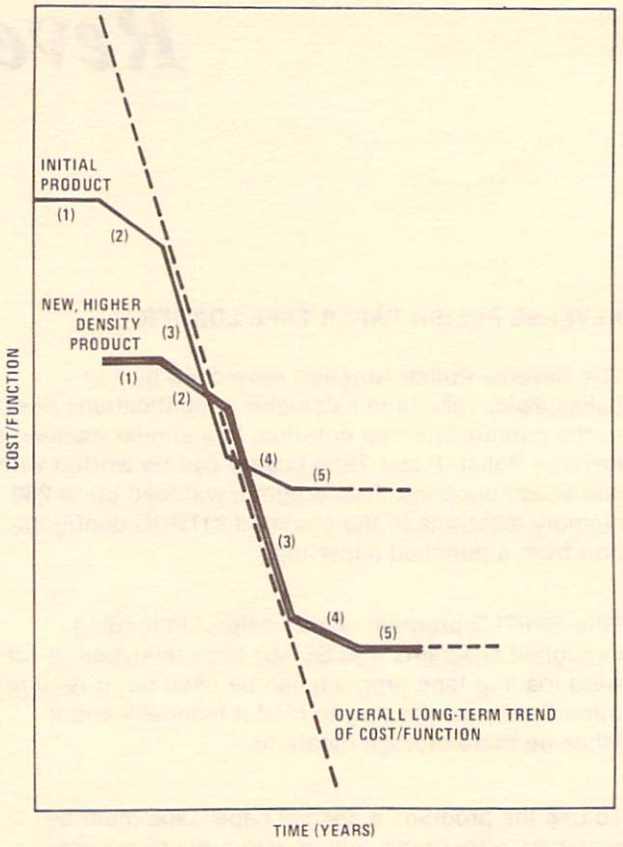
However, to go to a higher level of integration, which in case of Random Access Memory circuits, usually means a four-fold increase in number of bits on the chip, a significant improvement in batch density is required, otherwise no benefit is derived *(Figure 1)*.

This batch density (i.e., number of potentially good storage elements processed together as a single unit, such as a silicon wafer,) has shown an even higher rate of growth than the much more visible increase in the number storage bits/memory circuit.

During the past eight years the number of potentially good storage elements contained on a single silicon wafer has risen from about 50,000 to over 6 million, with the cost of processing a wafer rising only very slowly and manufacturing efficiency expressed as the percentage of good units staying level or improving slightly.

Future progress in memory technology can be examined in terms of this single variable common to all present and future solid state memory technologies.

There are several technological trends that are unfolding right now which are likely to impact future memory technology developments.



NOTES:

(1) Product is introduced, very little or no competition.

(2) Product is multiple sourced but prices still hold up as production is limited.

(3) Production expands dramatically as yields improve, competition is fierce, prices tumble, marginal suppliers are beginning to drop out.

(4) Significant yield improvements are no longer available, new product is beginning to compete for the same market, competition is still intense, suppliers still drop out..

(5) Major market share is taken by new generation of product, market shrinks but prices hold up as competition is minimal.

FIGURE 1. Typical Decrease of Memory Products' Prices/Costs During Product Life

These trends can be classified under the following categories:

a. Continued evolutionary process of memory cost reduction through more advanced circuit and device design techniques and improved process and manufacturing efficiencies.

b. A significant change in device and circuit sizes through major changes in pattern definition technology and an electrical scaling of devices to take advantage of the size reduction.

c. Charge Coupled Device and Magnetic Bubble Domain device based memory technologies.

a. EVOLUTIONARY PROCESS

This approach has so far been the most successful and continued improvements may still be expected. In fact, as long as this is a viable path for future development, it is likely to be the most vigorously pursued approach.

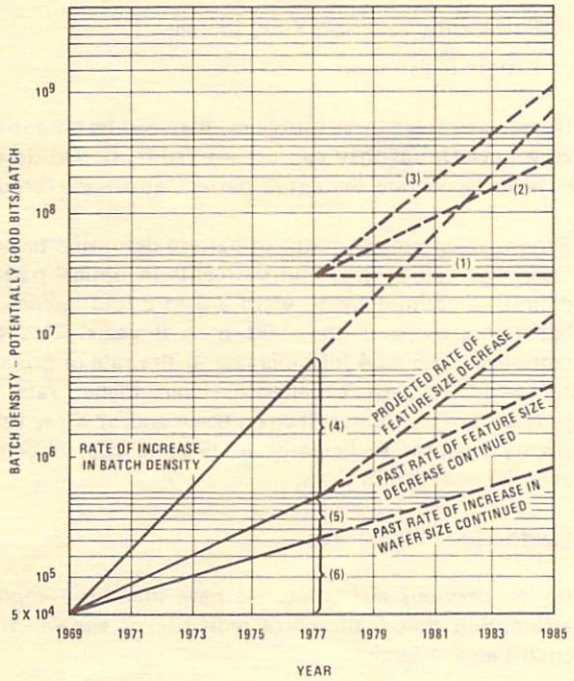
In terms of its future potential, we might examine past contributions to batch density improvements.

The total batch density improvement of 120-fold in eight years was contributed by:

1. Higher bit density through design and process innovation: 13.5x
2. Larger wafer area: 4x
3. Smaller feature sizes and tighter alignment tolerances: 2.2x

Continued improvement based on comparable contributions from the same sources is no longer feasible for the following reasons:

Design and process improvements, the most profitable source of past batch density improvement, is getting sufficiently close to its theoretical limits so that progress in it is likely to slow down *(Figure 2)*. It is clear that regardless of whatever technique we use to design or build a memory cell, it must have at least 2 features in both x and y directions, one to store the information and one to separate it from the adjacent cell. This defines a theoretical minimum cell size of 4 f^2 where f is the minimum feature size determined by the limits of pattern definition technology.



NOTES:

(1) Theoretical limit, current wafer and feature sizes.

(2) Theoretical limit, assuming continued improvements in wafer size increase and feature size reduction.

(3) Theoretical limit, assuming constant rate of wafer size increase and an *increasing* rate of feature size reduction.

(4) Increase due to design and process innovations.

(5) Increase due to feature size improvement.

(6) Increase due to wafer size.

FIGURE 2. Past and Projected Contributions to Batch Density Improvements

Cell size eight years ago was a rich 200 f^2 leaving plenty of room for improvement. Today's cell size of 20 f^2 or less is sufficiently close to the theoretical limit of 4 f^2 that we can no longer project a rate of improvement comparable to past norms. We will do extremely well if we can extract a further 3-fold improvement.

Wafer size improvement will continue at an essentially constant rate. Wafer size increases are important not only for increased productivity, but wafer size is strongly correlated to maximum economically manufacturable die size *(Figure 3)*. Wafer diameter has been increasing at a rate of about 1.4 times every four years. This rate of increase is tied not only to the rate at which equipment manufacturers can develop new tooling to handle the larger wafer size, but also to the rate at which capital is invested in the semiconductor industry.

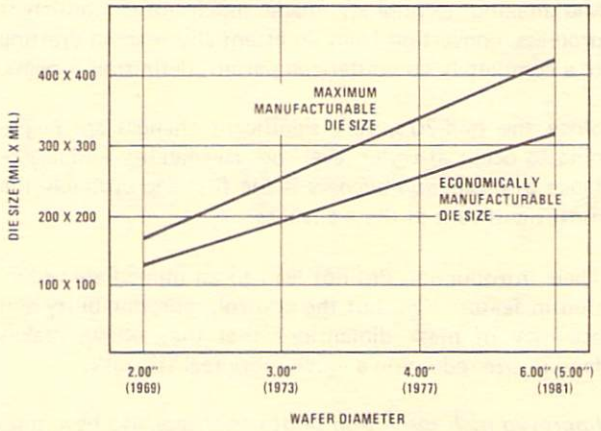


FIGURE 3. Maximum and Economic Die Size as a Function of Wafer Diameter (Time)

Feature size reduction. While we expect significant progress in this area, little of it can be considered evolutionary. In the past, progress in this area was completely evolutionary, contributing relatively little to density improvement. In the next 5 to 10 years we expect major changes in the technology and we will discuss those changes in detail later.

We also expect that manufacturing yields will increase in the next 5 to 10 years. This will be a factor in cost reduction but not in density.

The reason for yield improvement is the expected reduction in the rate of density improvement due to design and process improvements. Present manufacturing yields which include losses in wafer manufacturing, die sort, assembly and final test vary from under 5% for a leading edge product to about 25% for a mature product.

In the past, as long as significant density improvements were available from design and process innovations, engineering effort and talent was better utilized in trying to improve a new high density product's yield from 5% to 25%. Trying to extract the yield improvement available between 25% and 50%–60% which is probably the practical upper limit for any semiconductor product, was both harder and less rewarding. With less potential improvement available from design and process innovations, we can probably expect higher overall yields for mature products.

In summary, the evolutionary trend, while it will still contribute significantly to future cost reductions, will contribute proportionately less than it has in the past.

b. FEATURE SIZE IMPROVEMENT

Minimum feature size has been remarkably stable over the past 20 years of integrated circuit technology development. This was probably due to the fact that there was very little change in pattern definition technology. Up to 1975 the pattern definition technology, at least at wafer level, was basically unchanged from what it was in the late 50's and progress was obtained by better engineering, controlling and understanding the process and using improved photochemical materials.

Maskmaking technology made much more consistent progress, converting from an essentially manual drafting to a completely computerized pattern definition process.

Since the mid-70's, very significant changes are beginning to occur at wafer level too. Availability and acceptance of *projection aligners* is the first and probably the most significant of these changes.

Their introduction did not lead to an immediate reduction in feature size, but the control, reproducibility and accuracy of mask dimensions that they allow, makes feature size reduction a much more realistic task.

Improved high resolution photoresists are also becoming available.

Dry etching techniques are important technological achievements and will also be contributing to feature size reduction.

Electron beam and X-ray lithography are the most frequently mentioned technologies to achieve significant reductions in feature size.

There is undoubtedly significant progress being made in these areas and some of the results are impressive. However, they have to overcome some very significant technical and economic hurdles before they can make an impact on memory technology *(Figure 4)*.

Electron beam writing techniques are already available for maskmaking purposes where they offer some very real advantages. For direct writing on wafers, however, they still have to improve significantly and come down in price before they can make an impact on memory technology. Presently, projected machine costs and throughput times are such that processing wafers with electron beam writing instead of conventional masking—assuming no other technical problems—would raise wafer processing cost by a factor of 5. This cost increase would take care of all cost reduction achieved by the smaller feature size at *equal yield*. Since the smaller feature size means more densely built circuits sensitive to much smaller defect sizes the most immediate consequence of feature size reduction is yield reduction.

X-ray lithography techniques have still to resolve three basic problems.

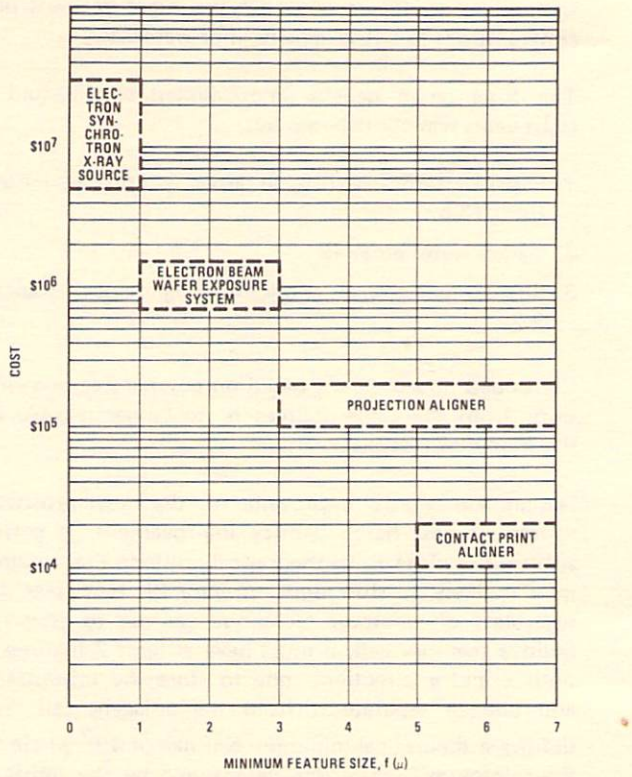


FIGURE 4. Cost of Key Equipment for Various Pattern Definition Technologies and Minimum Feature Sizes

a. Maskmaking technology

b. Sufficiently intensive X-ray sources

c. Pattern registration

If they can solve these problems, they can be potentially very powerful as they can use a fixed mask and do not have to regenerate the entire pattern at every exposure.

Summarizing present status of pattern definition technologies, we can project improvements in optical pattern definition technology to yield a 5 to 8-fold increase in batch density over the next 5 to 8 years. This will represent a 2.5 to 4-fold increase in the rate of progress compared to past experience. Even higher rates of progress are possible if electron beam and/or X-ray lithography matures sufficiently to become cost effective, over the next 5 to 8 years.

Electrical Scaling Devices

In the previous discussion, we have made the implicit assumption that feature size reduction is equivalent to circuit area reduction.

This is most certainly not the case. Feature size reduction will merely define limits to circuit size reduction. The actual reduction available will be determined by how closely the electrical device and circuit characteristics allow us to approach the limits imposed by pattern definition technology.

All three presently used major memory technologies (i.e., MOS dynamic, MOS static and bipolar static) are more limited by device and circuit design considerations, rather than optical pattern resolution.

In case of MOS devices, their performance is a function of the operating voltages and their ability to handle high operating voltages decreases very rapidly with reduced device sizes. Consequently, if denser memory circuits were to be built by taking advantage of feature size reduction, the operating voltages will have to be reduced. The resulting device and circuit performance reduction can be regained by re-engineering the entire device, reducing oxide thickness, junction depth and increasing substrate doping to make the device deliver an equivalent performance at lower operating voltages.

This total re-engineering of device structure, processing and manufacturing technology is called "scaling" and it is obviously a major engineering and manufacturing task, involving all aspects of wafer technology.

Bipolar memory circuits do not appear to suffer from this limitation; their's is, however, a different one. Device sizes can be reduced but their density cannot be significantly increased, because current drain of a bipolar device does not scale with size. Consequently, any attempt to take advantage of reduced device size by increasing number of bits/chip will run into severe power dissipation limits. Again the problem is technically solvable at an expense of major circuit design/process re-engineering efforts to "current scale" bipolar device/process technology.

I^2L technology appears technically attractive from this point of view (i.e., it would be able to take advantage of feature size reduction with the least amount of device and/or process engineering changes). Its problem is that it has so far not been able to establish a sufficiently attractive price/performance combination to gain a significant position in the memory market.

Feature size reduction and the required electrical scaling of devices will have some very important consequences in terms of relative impact on various memory technologies. When we scale devices, we adjust some basic device parameters and operating voltages so as to obtain as nearly identical device and circuit characteristics as possible. This can be achieved quite successfully for the type of circuits whose design is by and large based on the device characteristics that we have scaled (i.e., MOS static devices). For these devices, reduction of supply voltage also brings about a reduction in power dissipation, so one limitation to higher density, characteristic of static devices has also been removed.

MOS dynamic circuits, which have traditionally enjoyed a 4:1 density advantage over static devices, rely more on second order effects like leakage currents, subthreshold conduction and signal to noise ratio in their sense amplifier designs and do not benefit quite as readily from scaling.

Leakage current, whose relation to stored charge is vitally important to the successful operation of MOS dynamic random access memory circuits, does not scale proportionately with voltage, due to the point defect nature of the leakage current. Typically any junction's leakage current represents a spatial averaging over a relatively large number of defects. Reducing junction area will increase fluctuation in number of defect sites from one storage area to the next. Since dynamic RAM design requires that *all* storage areas have less than certain pre-determined amount of leakage current, scaling will typically reduce ratio of stored charge to leakage current. Since the signal available is already reduced by both scaling and the resulting increase in density, designers of future generation of dynamic RAMs face some formidable challenges. It is possible that the only way they will be able to overcome these challenges is to impose very strict environmental limitations on the finished product, namely cooling or even refrigeration of memory systems.

Feature size reduction and electrical scaling will impose some very stringent demands on process engineering in terms of both control and the degree of perfection required for good yields from the scaled structures. We are assuming that these problems are solvable by evolutionary improvements in processing techniques. We should not be surprised, however, if progress in those areas from time to time fails to keep up with the more visible improvements available from pattern definition technology.

c. NEW TECHNOLOGIES

Success in semiconductor integrated circuit based random access memory technology prompted considerable interest in solid state replacements for serial memories. The two most often considered candidates are Charge Coupled Devices and Bubble Domain Memory devices.

Charge Coupled Devices represent the densest silicon based technology we know. However, their speed and ease of use is considerably inferior to random access memories and as long as random access memories can be made with comparable circuit density, C.C.D. is hard pressed to carve out a market position. Typically, for a C.C.D. circuit to be competitive with RAMs, it has to offer a 4:1 density advantage over a comparably sized RAM circuit. So far it has not been able to do it, partly because RAM technology very quickly adopted all process improvements made for C.C.D. circuits and used them to make competitively sized RAMs.

However, C.C.D. technology is expected to establish a 4:1 density advantage over RAMs in the reasonably near future because its technology and organization permits:

a. Approaching the theoretical minimum storage area of 4 f^2 both more easily and more closely than RAMs.

b. Meeting the challenges of feature size reduction and device scaling more easily than dynamic RAMs.

Several features of C.C.D. technology contribute to these advantages. Absence of P-N junctions allows storage and transfer functions to be very similar structurally and either very closely spaced, or used interchangeably for both functions.

Although charge is stored dynamically, it is not held at any location for longer than a clock cycle so effect of defect density fluctuation is averaged out over a large area. Signal strength is comparable to RAMs but there is more flexibility in sense amplifier design. Absence of contacts and P-N junctions allows more efficient layout and easier scaling of devices.

Bubble Memory Technology

Although Bubble Memory technology is significantly different from CCD technology, it is also based on a batch manufacturing process with the cost of a function very strongly dependent of the functional density per batch and manufacturing yields.

Examined from this point of view, it has some very major disadvantages coupled with some even greater potential long-term benefits.

First of all, a Bubble Memory device is very well suited to serial storage of data. Although it is slower than any silicon I. C. based storage circuit, it is non-volatile—or at least it can be designed to be—and it can also be used to perform very simple logic functions which allow data to be stored and retrieved efficiently. Also, it can be used to pre-amplify the otherwise very small signal magnetically so it can be used to design a reasonably self-contained memory chip.

Its known major disadvantages are:

1. Very high material cost, caused by both very high initial substrate cost and a very costly, difficult and low productivity liquid phase epitaxy deposition process. Material cost is 30–50 times higher than silicon.

2. Very high packaging cost. Every circuit has to have an individually adjusted bias field and a rotating magnetic field built into the package.

3. A batch density which is presently not significantly higher than what is achievable with silicon.

Set against these disadvantages we can consider the potential long-term benefits which motivate the ever increasing activity in the field:

1. Processing typically requires only 3 masking steps, only one of which is critical, compared to 6+ for silicon.

2. Although present bit density is not impressive, it is based on a relatively simple design with bit area being in the 200 f^2 region for a T bar configuration, indicating very much room for improvement, some of which has already been implemented experimentally.

3. Because it has only one critical masking step and no critical alignment requirements, it is the technology best positioned to take advantage of improvements in pattern definition techniques.

It is difficult today to determine the point both in time and in level of complexity at which Bubble Memory Devices will be able to enter the market and compete successfully. But once they do, they will enjoy a very rapid growth comparable to silicon integrated circuit based memory circuits for exactly the same reasons.

Summarizing these trends, there is sufficient visibility for the continued technical progress of memory technology at essentially unchanged rates for the next 5 to 8 years.

One word of caution, however, is worth mentioning here. The key to past success and the continued objective of memory technology development is *cost reduction*.

Technical developments to continue to increase density of memory circuits are worthwhile only if they can make a significant contribution to this overall objective. They cannot do it if the cost of improvement is so high that it swallows up all future cost benefits.

Even if their cost is less than potential cost reduction benefit, they still represent a very significant investment in design, process development, production and testing facilities and product start-up costs for the component manufacturer.

Such an investment will only be economically attractive if the market for memory products continues to expand at a fast rate.

EDITORIAL

Thank you for returning your qualification forms. Sometime this month you will be sent the SC/MP and/or 8080 Quick Reference Guides that you requested.

We are now publishing bigger issues of COMPUTE every other month. Any comments on our format are always appreciated by our editors.

About articles, two things — First, articles that are published in COMPUTE entitle the author(s) to either a National Semiconductor watch or calculator. When submitting an article, please specify whether you wish to receive a men's or women's LCD watch or calculator. Second, we will try to acknowledge receipt of your article within two weeks and we need to have your name, address and phone number as part of the article.

The user library is always in need of new programs. We are particularly looking for 8080, 8060 (SC/MP) and 8900 (PACE) programs. The major requirement is that we need a copy of the source program (for distribution and/or publication). We can accept these programs on PACE UDS diskettes or paper tape. We will return the diskette, if requested. A library program submittal will also earn you a National watch or calculator.

In this issue we are including a consultant list. These firms or individuals have expressed either an interest in supporting National Semiconductor's microprocessor products or have successfully supported our customers in the past. We will be aggressively supporting selected consultants and need your help. If you have had a successful experience with any of these listed consultants, let us know. If you need help on any of your microprocessor related projects, call us and we can recommend a firm in your area.

Lastly, we have a microprocessor university/college support program. Any high school teachers, college or university professors who would like information on this program should contact us. We will mail them a university pamphlet explaining the program. We also are initiating a visiting professor program for teachers on leave, sabbatical or vacation who want to learn about microprocessors. Contact us if you are one of these guys or gals.

Georgia

SC/MP KEYBOARD KIT DISPLAY

by B.T. Larkin

The SC/MP Keyboard Kit is capable of showing almost any of the letters of the alphabet on its eight-place, seven-segment LED display. No changes are required in the keyboard kit.

At present, the keyboard permits direct keying of the letters A-F and any of the decimal digits. A short display program (Appendix C, SC/MP Keyboard Kit Users Manual) also permits showing the alphabetic text, "did Good", the letters being entered in hexadecimal code.

This display program has now been generalized so that most of the alphabet, all of the decimal digits, and some miscellaneous characters can be shown. The character codes are listed in Table 1. For convenience, the generalized program is also presented, along with some trial programs (Tables 3a and 3b).

The complete sequence of character codes generated by the SC/MP Keyboard Kit is listed in Table 2 for those who may wish to complete an alphabet with the best remaining seven-segment characters. Such an alphabet is already in use on at least one other single-board computer.

The display program (Table 3a) may prove useful within a larger program as means of expanding the data output of the SC/MP Keyboard display.

Table 1. Characters Available on Unmodified SC/MP Keyboard Display[1]

CHAR	HEX	DISPLAY	CHAR	HEX	DISPLAY
A	77	A	a	5F	a
B			b	7C	b
C	39	C	c	58	c
D			d	5E	d
E	79	E	e	7B	E
F	71	F	f		
G	3D	G	g	6F	g
H	76	H	h	74	h
I	06	I	i	10	i
J	1E	J	j		
K			k		
L	38	L	l	06	I
M			m		
N			n	54	n
O	3F	O	o	5C	o
P	73	P	p		
Q			q		
R			r	50	r
S	6D	S	s		
T			t	78	t
U	3E	U	u	1C	u
V			v		
W			w		
X			x		
Y	6E	y	y	6E	y
Z			z		

Table 1. Characters Available on Unmodified SC/MP Keyboard Display[1] (continued)

CHAR	HEX	DISPLAY	CHAR	HEX	DISPLAY
0	3F	0		00[2]	
1	06	1		39	C
2	5B	2		8F	J
3	4F	3		48	=
4	66	4		08	-
5	6D	5		40	-
6	7D	6		01	-
7	07	7		30	I
8	7F	8		06	I
9	67	9		02	

(1) Using the display program in Appendix C, SC/MP Keyboard Kit Users Manual.

(2) "00" will erase any individual seven-segment display.

Table 2. Complete Sequence of Seven-Segment Display Codes for SC/MP Keyboard Kit[1]

	0	1	2	3	4	5	6	7	8	9	A	b	C	d	E	F
0		-	'	¬	,	¯	/	7	_	¯	_'	_¬	⌟	¯	⌟	⌟
1	,	,-	,'	,¬	,,	,¯	,/	,7	⌞	⌞¯	⌞'	⌞¬	⌞⌟	⌞¯	⌞⌟	⌞⌟
2	'	⌜	''	⌜¬	',	⌜¯	'/	⌜7	⌞	⌜¯	''	⌜¬	'⌟	⌜¯	'⌟	⌜⌟
3	/	⌜	/'	⌜¬	/,	⌜¯	//	⌜7	⌞	⌜¯	/'	⌜¬	/⌟	⌜¯	/⌟	⌜⌟
4	-	=	⌟	⌐	¬	¯	¬/	¬7	=	=	⌟	⌐	⌐	¯	⌟	⌐
5	⌜	⌜¯	⌜⌟	⌜¬	⌜¬	⌜¯	⌜⌟	⌜¬	⌜¯	⌜¯	⌜⌟	⌜¬	⌜¬	⌜¯	⌜⌟	⌜⌟
6	⌞	⌞¯	⌞⌟	⌞¬	⌞¬	⌞¯	⌞⌟	⌞¬	⌞¯	⌞¯	⌞⌟	⌞¬	⌞¬	⌞¯	⌞⌟	⌞⌟
7	⌜	⌜¯	⌜⌟	⌜¬	⌜¬	⌜¯	⌜⌟	⌜¬	⌜¯	⌜¯	⌜⌟	⌜¬	⌜¬	⌜¯	⌜⌟	⌜⌟
8		-	'	¬	,	¯	/	7	_	¯	_'	_¬	⌟	¯	⌟	⌟

(1) The placing of display segments is quite regular, and is governed by five superimposed rules. This generates 128 differing segment combinations. The series is complete from 00-7F, and repeats in full from 80-FF. There are thus two effective codes for every character desired.

Table 3a. Display Program for SC/MP Keyboard Kit[1]

	KEY
Part 1	Initiate
	Mem
	F,F,b
	Term
	F
	Term,Mem,Term
	2,0
	Term
	F,2,0
	Term
Part 2	Enter the desired character codes (digit pairs) in reverse sequence. Follow each pair with "Term,Mem,Term", except after the last pair ("Term" only). Program accepts up to eight characters or spaces at a time.
Part 3	Go,Go
	1,8,5
	Term (Display appears now).

(1) Based on the original display program in Appendix C, SC/MP Keyboard Kit Users Manual.

Table 3b. Trial Display Programs

Program each series from right to left to reverse pair order. Key in "Term,Mem,Term" after each pair except for the last ("Term" only).

1)	1E,	3E,	38,	6E,	00,	66,	78,	74	(Date)
2)	00,	07,	40,	4F,	48,	66,	00,	00	(Equation)
3)	00,	00,	76,	79,	38,	38,	3F,	00	(Greeting)
4)	00,	6d,	76,	79,	06,	38,	77,	00	(Name)
5)	40,	01,	40,	08,	40,	01,	40,	5C	(Whimsy 1)
6)	01,	01,	01,	40,	08,	08,	01,	01	(Whimsy 2)

Muxing It Up

A new low-power CMOS device incorporates a 16-channel multiplexer, a chopper stabilized comparator, an 8-bit analog-to-digital converter, a TRI-STATE® latched output buffer and all control logic housed in a 40-pin dual-in-line package. The device, essentially a complete data-acquisition system on a monolithic chip, requires only a single 5-volt supply and consumes 15 milliwatts, worst case. Pricing, in 100 unit quantities, is $19.95 each.

Designated the INS8292, the device is one of National's expanding line of INS8080A microprocessor peripheral control, digital I/O, communications and memory support products. These support devices interface with National's universal MICROBUS system, a concept that incorporates complete data, address and control bus functions. Using the MICROBUS, a designer is assured that all devices are compatible with few or no external circuits required.

The INS8292 single-chip data-acquisition system is ideal for process-, industrial- and machine-control applications where high accuracy, high speed and low power are essential.

The 16-channel multiplexer accepts single-ended analog signals from ratiometric sensors such as potentiometers, strain gauges, thermister bridges, pressure transducers and other transducers where the change in value is measured instead of absolute value.

Designed for application flexibility, the multiplexer output is pinned out, as is the comparitor input. This subtle feature permits channel expansion using other multiplexers into the INS8292 A/D converter. It also accommodates signal conditioning such as pre-scaling, sample and hold, signal preamplification, and standard-signal insertion for absolute measurements.

The A/D converter uses successive approximation techniques through a 256-step (256R) register-ladder network rather than the conventional two-value network (R/2R). This procedure provides consistent reference-voltage loading, eliminates missing conversion codes and prevents feedback in closed-loop systems.

For more information contact:

Marketing Services/MS520
(408) 737-5142

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DISTRIBUTED MICROCOMPUTERS
CONTROL HYDROELECTRIC PLANT, REMOTELY

A distinguished trio of microcomputer systems is remotely monitoring meteorological conditions, controlling water flow, and managing electric power generation on a hydroelectric project along the Alabama River.

The compact and low-cost system allows the Army Corps of Engineers to operate the entire Jones Bluff Hydroelectric Project, including four 17-megawatt generators, from the control room of another river project at Millers Ferry, some 90 miles away.

Remote operation of the plant is saving about five man-years annually, while the use of microcomputers instead of a more conventional design employing hardwired logic, or a design built around a minicomputer system, has saved thousands of dollars in system development, hardware and installation costs.

DISTRIBUTED SYSTEM CONFIGURATION

Essentially, the systems, using three 16-bit IMP-16C/200 microcomputer cards, function as a distributed computer network. Each of the three has a specific role to play — one system performs data acquisition, a second handles plant control, and the third is the central supervisory unit at Millers Ferry.

SYSTEM MONITORS AND CONTROLS DAM GATES AND GENERATORS

Using the three IMP-16 systems, the operator of the Jones Bluff Hydroelectric Project receives and has displayed before him 25 separate data readings which are updated every two seconds. Control functions such as opening or closing the large concrete dam gates, or altering the generator outputs are executed by merely setting a switch or dial at Millers Ferry. The central supervisory microprocessor controls communication to and from Jones Bluff over a microwave system. The microcomputer is also connected to a nearby display unit and to the Millers Ferry central minicomputer primarily for producing summary tabulations of dam operations.

The Jones Bluff project is located on the Alabama River about 35 miles from Montgomery. The $55 million project, completed in September 1976, produces an average annual energy output of 329,000,000 kilowatt hours.

SYSTEM OPERATION

Two National Semiconductor microcomputer boards are located at Jones Bluff, one for data acquisition; the other for operating control. Information sensed at the four generators and at the dam is passed in digital form via a microwave communications system to the supervisory unit at Millers Ferry.

The microwave link, which is used to convey control signals as well, uses 300-baud modems and a repeater station where multiplexed signals (7-8 gigahertz) are regenerated.

The microprocessors code and decode the multiplexed signals sent over the microwave link, thus permitting a single channel to handle the entire information transfer.

As communications processors, the IMP-16s set line-protocol administration; assemble messages; check syntax, and detect errors not only among themselves but also with a Millers Ferry minicomputer.

For more information:

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Sid Clack
5160 N. Lagoon Avenue
Portland, Oregon 97217
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U.S. Army Corps of Engineers
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